

SM4503NHKP-VB Datasheet N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)			
30	0.003 at V _{GS} = 10 V	120	71 nC			
30	0.005 at V _{GS} = 4.5 V	90	71110			

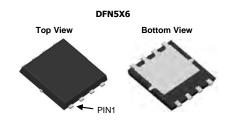
FEATURES

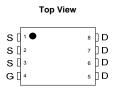
- Trench Power MOSFET
- 100 % R_g and UIS Tested

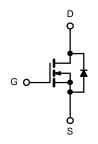


APPLICATIONS

- Notebook PC Core
- VRM/POL







N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V_{GS}	± 20	v	
	T _C = 25 °C		120 ^{a, e}		
Continuous Prain Current /T = 175 °C)	T _C = 70 °C		90 ^e		
Continuous Drain Current (T _J = 175 °C)	T _A = 25 °C	I _D	21 ^{b, c}	A	
	T _A = 70 °C		20.8 ^{b, c}	^	
Pulsed Drain Current		I _{DM}	250		
Avalanche Current Pulse	L = 0.1 mH	I _{AS}	56		
Single Pulse Avalanche Energy	L=0.1 IIII	E _{AS}	60	mJ	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	80 ^{a, e}	А	
Continuous Source-Diam Diode Current	T _A = 25 °C	'S	76 ^{b, c}	_ A	
	T _C = 25 °C		210 ^a		
Maximum Power Dissipation	T _C = 70 °C	P _D	155	W	
Maximum Power Dissipation	T _A = 25 °C	' D	35 ^{b, c}	VV	
	T _A = 70 °C		13 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R_{thJA}	41	50	°C/W		
Maximum Junction-to-Case	Steady State	R _{thJC}	0.7	0.9	C/VV		

Notes:

- a. Based on T_C = 25 °C. b. Surface mounted on 1" x 1" FR4 board.
- d. Maximum under steady state conditions is 90 °C/W.
- e. Calculated based on maximum junction temperature. Package limitation current is 80 A.



Parameter	Symbol	Test Conditions	Min .	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		35		m\//°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	1 _D = 200 μΛ		- 5.5		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zara Cata Valtaga Drain Current	1	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	80			Α
	Б	$V_{GS} = 10 \text{ V}, I_D = 32 \text{ A}$		0.003		Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 29 \text{ A}$		0.005		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 32 A		130		S
Dynamic ^b						•
Input Capacitance	C _{iss}				3200	pF
Output Capacitance	C _{oss}	V_{DS} = 12.5 V, V_{GS} = 0 V, f = 1 MHz			1025	
Reverse Transfer Capacitance	C _{rss}				970	
Total Gate Charge	Q _g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 32 \text{ A}$			71	nC
					61.5	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 29 \text{ A}$			34	
Gate-Drain Charge	Q_{gd}				29	
Gate Resistance	R _g	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t _{d(on)}			18	27	ns
Rise Time	t _r	V_{DD} = 15 V, R_L = 0.555 Ω		11	17	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 27 A, V_{GEN} = 10 V, R_g = 1 Ω		70	105	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}			55	83	
Rise Time	t _r	V_{DD} = 15 V, R_L = 0.625 Ω		180	270	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 24$ A, $V_{GEN}=4.5$ V, $R_g=1$ Ω		55	83	
Fall Time	t _f			12	18	
Drain-Source Body Diode Characteristic	es					•
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			80	۸
Pulse Diode Forward Current ^a	I _{SM}				100	A
Body Diode Voltage	V _{SD}	I _S = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			52	78	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$I_F = 20 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		70.2	105	nC
Reverse Recovery Fall Time	t _a	i _F = 20 A, αι/αι = 100 A/μs, 1 _J = 25 °C		27		
Reverse Recovery Rise Time	t _b			25		ns

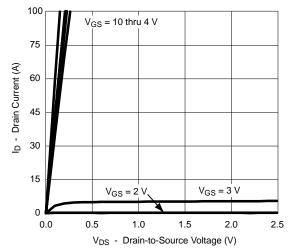
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

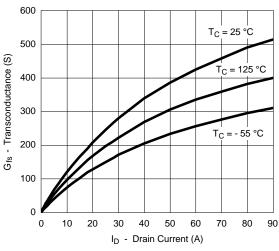
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



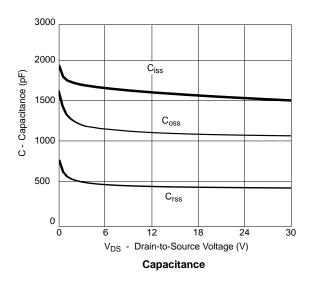
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

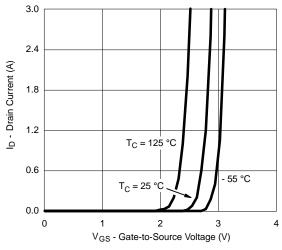


Output Characteristics

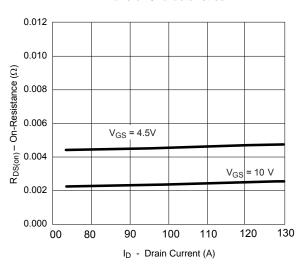


Transconductance

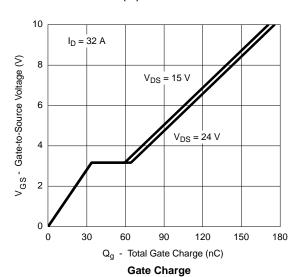




Transfer Characteristics

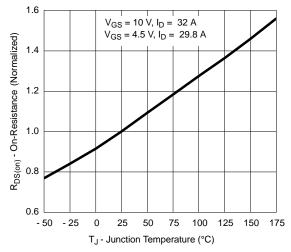


R_{DS(on)} vs. Drain Current

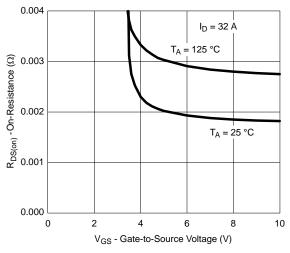




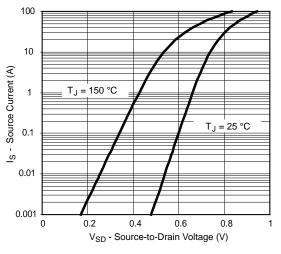
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



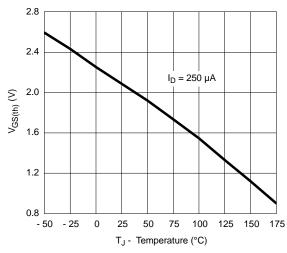
On-Resistance vs. Junction Temperature



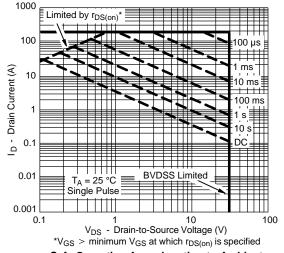
 $\rm R_{\rm DS(on)}$ vs. $\rm V_{\rm GS}$ vs. Temperature



Forward Diode Voltage vs. Temperature



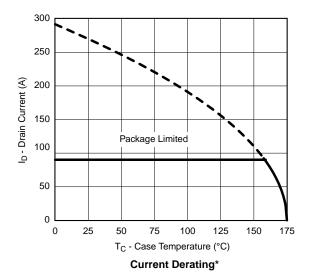
Threshold Voltage

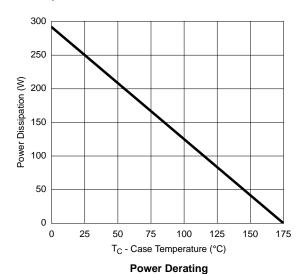


Safe Operating Area, Junction-to-Ambient

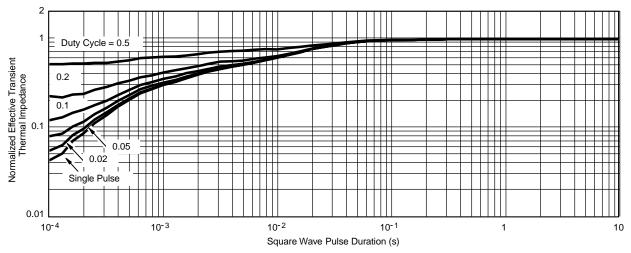


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





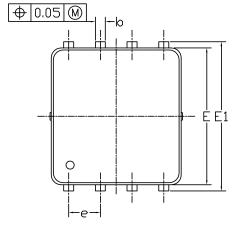
* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

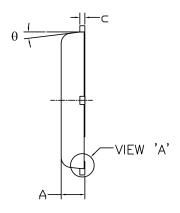


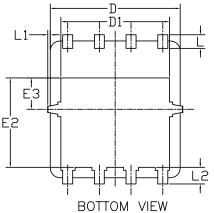
Normalized Thermal Transient Impedance, Junction-to-Case

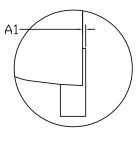


DFN5x6_8L_EP1_P PACKAGE OUTLIN



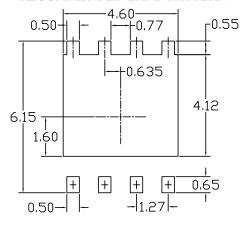






<u>VIEW 'A'</u> (SCALE 5:1)

RECOMMENDED LAND PATTERN



CVA (DOLC	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
SYMBOLS	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.85	0. 95	1.00	0.033	0.037	0.039	
Al	0.00		0.05	0.000		0.002	
b	0.30	0.40	0.50	0.012	0.016	0.020	
c	0. 15	0. 20	0. 25	0.006	0.008	0.010	
D	5. 10	5. 20	5. 30	0. 201	0. 205	0. 209	
D1	4. 25	4. 35	4. 45	0. 167	0.171	0. 175	
Е	5. 45	5. 55	5. 65	0. 215	0. 219	0. 222	
E1	5. 95	6.05	6. 15	0. 234	0. 238	0. 242	
E2	3. 525	3. 625	3. 725	0.139	0. 143	0. 147	
E3	1. 175	1. 275	1. 375	0.046	0.050	0.054	
e	1. 27 BSC			0.050 BSC			
L	0.45	0. 55	0.65	0.018	0.022	0.026	
L1	0		0. 15	0		0.006	
L2	0.68 REF			0.027 REF			
θ	0°		10°	0°		10°	

NOTE

- UNIT: mm
- 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- 2. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.



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