

### SIR838DP-VB Datasheet

## N-Channel 150 V (D-S) MOSFET

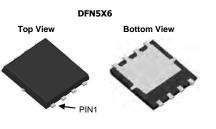
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A) <sup>g</sup>	Q <sub>g</sub> (Typ.)		
150	0.0158 at V <sub>GS</sub> = 10 V	53.7	22.8 nC		
	0.0188 at V <sub>GS</sub> = 7.5 V	45	22.0110		

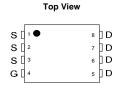
#### **FEATURES**

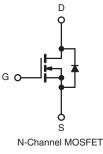
- Trench Power MOSFET
- 100 %  $R_q$  and UIS Tested

#### **APPLICATIONS**

- Fixed Telecom
- DC/DC Converter
- Primary and Secondary Side Switch ٠







Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	150	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
	T <sub>C</sub> = 25 °C		53.7		
Continuous Drain Current ( $T_1 = 150 \ ^{\circ}C$ )	T <sub>C</sub> = 70 °C	1-	43		
Continuous Drain Current (1j = 150°C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	12.8 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		10.2 <sup>b, c</sup>	A	
Pulsed Drain Current (t = 300 μs)		I <sub>DM</sub>	130		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	la la	60 <sup>a</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	5.6 <sup>b, c</sup>		
Single Pulse Avalanche Current		I <sub>AS</sub>	30		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	45	mJ	
	T <sub>C</sub> = 25 °C		104		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	PD	66.6	w	
	T <sub>A</sub> = 25 °C	' D	6.25 <sup>b, c</sup>	vv	
	T <sub>A</sub> = 70 °C		4 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		
Soldering Recommendations (Peak Temperature	e) <sup>d, e</sup>		260		

#### THEDMAL RESISTANCE BATINGS

I RENMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	15	20	°C/W		
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	0.9	1.2	0/11		

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. The DFN5x 6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 54 °C/W.

g. T<sub>C</sub> = 25 °C.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static		F	Γ		Г <u> </u>	T			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$	150			V			
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		105		mV/°0			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 9.4					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	2.0		4.0	V			
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V$ , $V_{GS} = \pm 20 V$			± 100	nA			
Zero Gate Voltage Drain Current	1200	$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA			
Zero Gale voltage Drain Gurrent	I <sub>DSS</sub>	$V_{DS}$ = 150 V, $V_{GS}$ = 0 V, $T_{J}$ = 70 °C			10				
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			А			
	Б	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0158	0.0158				
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 15 A		0.0188		Ω			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A		30		S			
Dynamic <sup>b</sup>		· · · · · · · · · · · · · · · · · · ·							
Input Capacitance	C <sub>iss</sub>			1286		pF			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz		327					
Reverse Transfer Capacitance	C <sub>rss</sub>			28					
·		V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		31.3	47	nC			
Total Gate Charge	Qg			22.8	35				
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A		8					
Gate-Drain Charge	Q <sub>gd</sub>			10					
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V		66	100				
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.3	1	2	Ω			
Turn-On Delay Time	t <sub>d(on)</sub>			10	20	-			
Rise Time	t <sub>r</sub>	$V_{DD}$ = 75 V, R <sub>L</sub> = 3.75 Ω		12	24				
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 20$ Å, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		15	30				
Fall Time	t <sub>f</sub>	-		7	14				
Turn-On Delay Time	t <sub>d(on)</sub>			12	24	ns			
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = 75 V, R <sub>I</sub> = 3.75 Ω		13	26	-			
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 20 \text{ A}, \text{ V}_{\text{GEN}} = 7.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		17	34				
Fall Time	t <sub>f</sub>	Ĩ		8	16				
Drain-Source Body Diode Characteristic			1	1	I	1			
Continuous Source-Drain Diode Current	ا <sub>S</sub>	T <sub>C</sub> = 25 °C			60	<u> </u>			
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	A			
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A		0.77	1.1	V			
Body Diode Reverse Recovery Time	t <sub>rr</sub>	-		95	190	ns			
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			280	560	nC			
Reverse Recovery Fall Time	t <sub>a</sub>	$I_{F} = 20 \text{ A}, \text{ dl/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_{J} = 25 \text{ °C}$		72					
Reverse Recovery Rise Time	t <sub>b</sub>			23		ns			

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

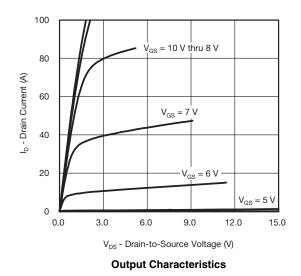
b. Guaranteed by design, not subject to production testing.

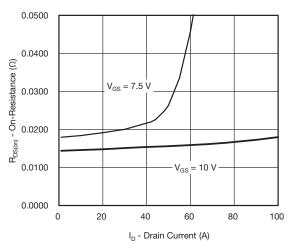
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bsemi

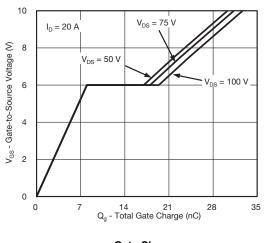
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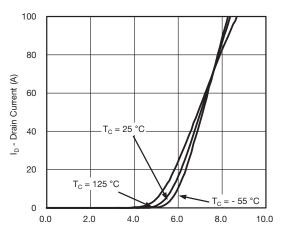




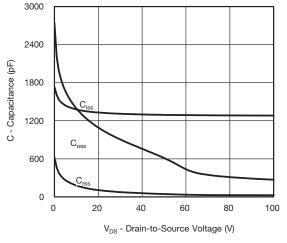
**On-Resistance vs. Drain Current** 



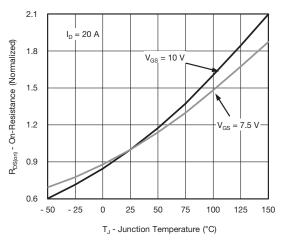
Gate Charge



V<sub>GS</sub> - Gate-to-Source Voltage (V) Transfer Characteristics

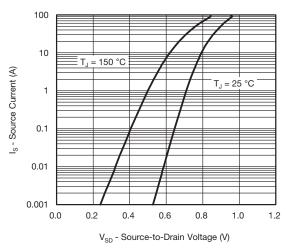


Capacitance

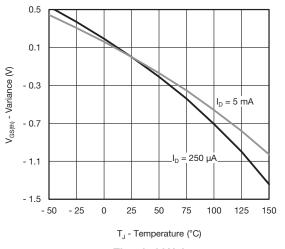


**On-Resistance vs. Junction Temperature** 

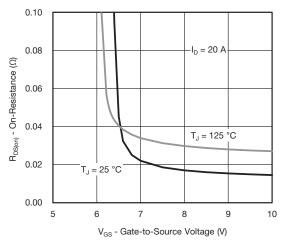




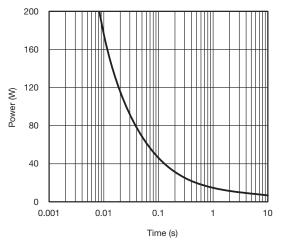




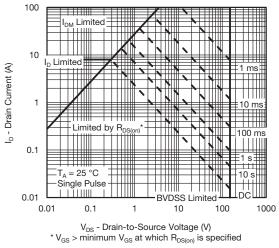
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage

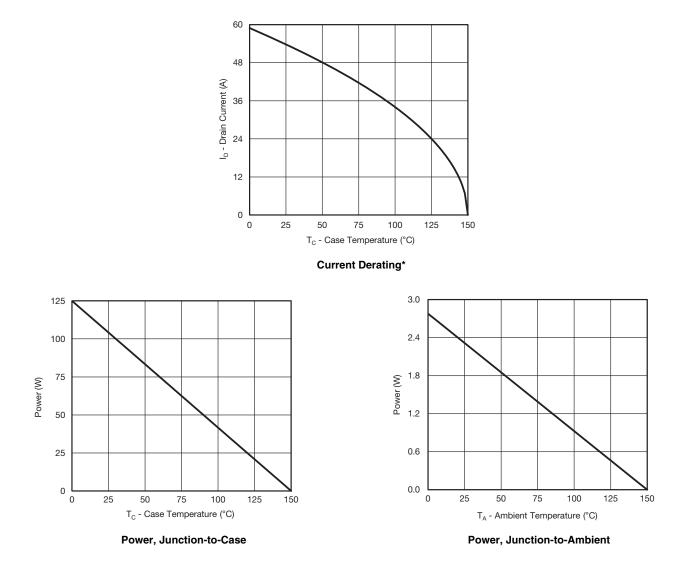


Single Pulse Power, Junction-to-Ambient



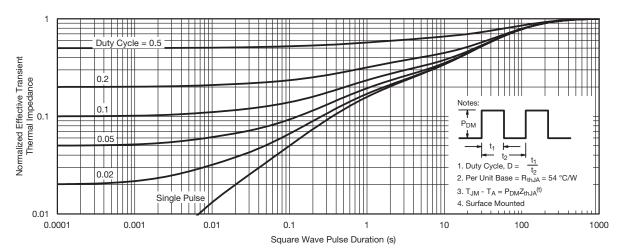
Safe Operating Area, Junction-to-Ambient



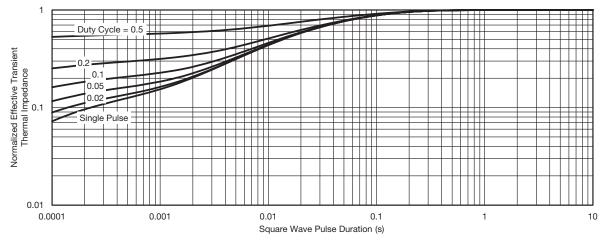


\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





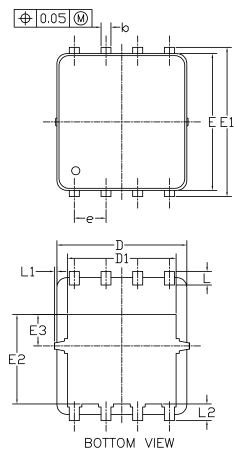
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

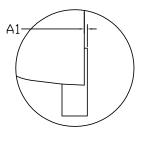






θ VIEW 'A'

Δ



<u>VIEW 'A'</u> (SCALE 5:1)

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.85	0.95	1.00	0.033	0.037	0.039	
A1	0.00		0.05	0.000		0.002	
b	0.30	0.40	0.50	0.012	0.016	0.020	
c	0.15	0.20	0.25	0.006	0.008	0.010	
D	5.10	5.20	5.30	0.201	0.205	0.209	
D1	4.25	4.35	4.45	0.167	0.171	0.175	
E	5.45	5.55	5.65	0.215	0.219	0.222	
E1	5.95	6.05	6.15	0.234	0.238	0.242	
E2	3.525	3.625	3.725	0.139	0.143	0.147	
E3	1.175	1.275	1.375	0.046	0.050	0.054	
e	1.27 BSC			0.050 BSC			
L	0.45	0.55	0.65	0.018	0.022	0.026	
L1	0		0.15	0		0.006	
L2	0.68 REF			0.027 REF			
θ	0°		10°	0°		10°	

NOTE

UNIT: mm

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.

MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH. 2. CONTROLLING DIMENSION IS MILLIMETER.

CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.



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