

## HM35P03D-VB Datasheet

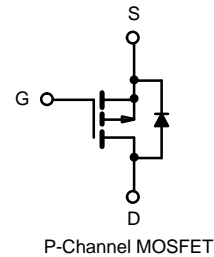
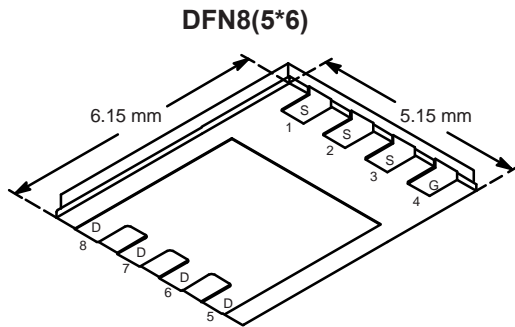
### P-Channel 30 V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D^a$	$Q_g$ (Typ.)
- 30	0.0080 at $V_{GS} = -10$ V	- 60	66 nC
	0.0090 at $V_{GS} = -6$ V	- 53	
	0.0120 at $V_{GS} = -4.5$ V	- 50	

#### FEATURES

- Extended  $V_{GS}$  range ( $\pm 25$  V) for adaptor switch applications
- Extremely low  $R_{DS(on)}$
- Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested


**RoHS**  
 COMPLIANT


#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	- 60	A
	$T_C = 70^\circ\text{C}$	- 50.7	
	$T_A = 25^\circ\text{C}$	- 47.3	
	$T_A = 70^\circ\text{C}$	- 43.9 <sup>b, c</sup>	
Pulsed Drain Current ( $t = 300 \mu\text{s}$ )	$I_{DM}$	- 150	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	- 58 <sup>b, c</sup>	
	$T_A = 25^\circ\text{C}$	- 46 <sup>b, c</sup>	
Single Pulse Avalanche Current	$I_{AS}$	- 40	mJ
Single Pulse Avalanche Energy	$E_{AS}$	80	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	75	W
	$T_C = 70^\circ\text{C}$	40	
	$T_A = 25^\circ\text{C}$	3.1 <sup>b, c</sup>	
	$T_A = 70^\circ\text{C}$	2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	33	40	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	15	17	

Notes:

 a. Based on  $T_C = 25^\circ\text{C}$ .

b. Surface mounted on 1" x 1" FR4 board.

 c.  $t = 10$  s.

 d. Maximum under steady state conditions is  $90^\circ\text{C/W}$ .

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 24		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			6		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1.0		- 2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 25 V			± 150	μA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 15	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	
		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 10 V	- 20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 13 A		0.0080		Ω
		V <sub>GS</sub> = - 6 V, I <sub>D</sub> = - 10 A		0.0090		
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8 A		0.0120		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 13 A		44		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4620		pF
Output Capacitance	C <sub>oss</sub>			880		
Reverse Transfer Capacitance	C <sub>rss</sub>			820		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 17.3 A		102	153	nC
				66	80	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 5 V, I <sub>D</sub> = - 17.3 A		16		
Gate-Drain Charge	Q <sub>gd</sub>			28		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.3	1.3	2.6	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 0 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		70	105	ns
Rise Time	t <sub>r</sub>			70	105	
Turn-Off Delay Time	t <sub>d(off)</sub>			45	68	
Fall Time	t <sub>f</sub>			27	41	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		18	30	
Rise Time	t <sub>r</sub>			15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			52	80	
Fall Time	t <sub>f</sub>			14	25	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 5.8	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 60	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 10 A, V <sub>GS</sub> = 0 V		- 0.78	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		35	53	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			25	38	nC
Reverse Recovery Fall Time	t <sub>a</sub>			19		ns
Reverse Recovery Rise Time	t <sub>b</sub>			16		

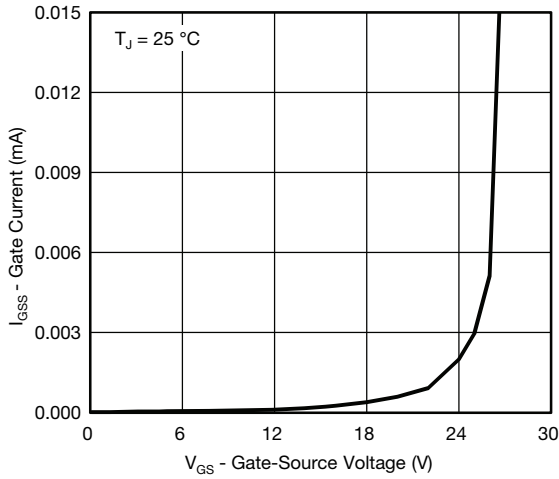
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ 

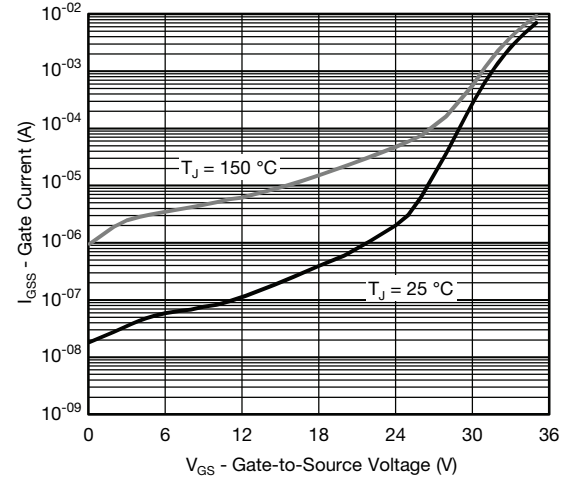
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

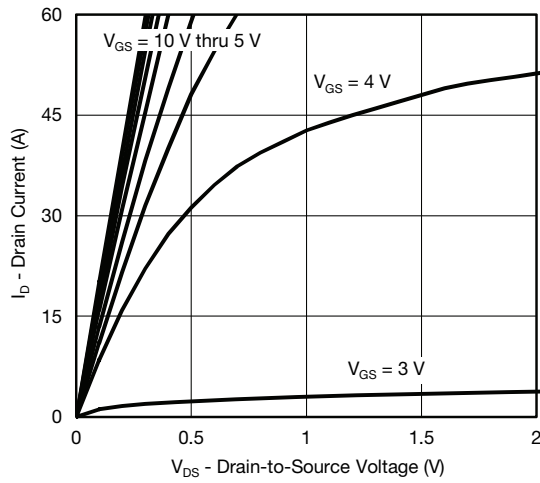
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



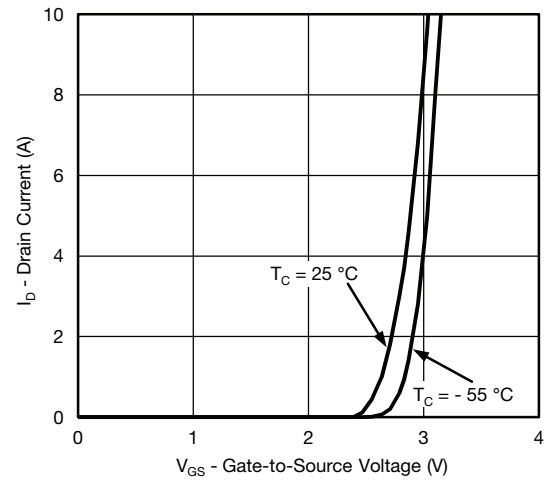
**Gate Current vs. Gate-Source Voltage**



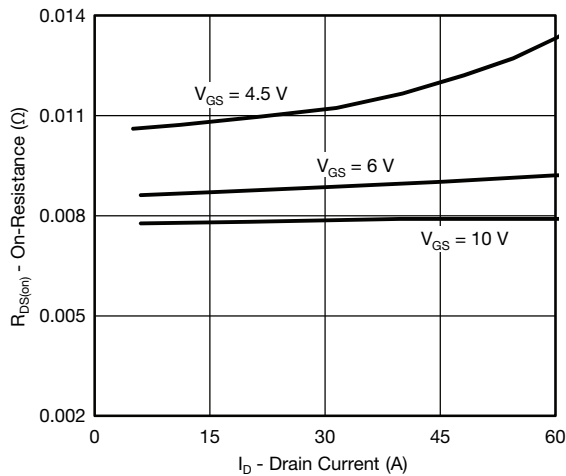
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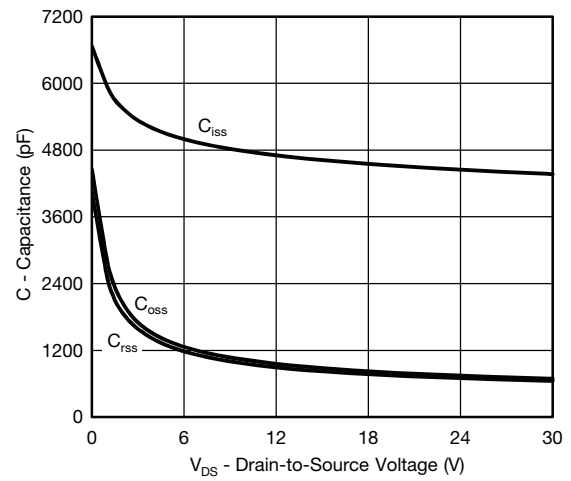
**Output Characteristics**



**Transfer Characteristics**

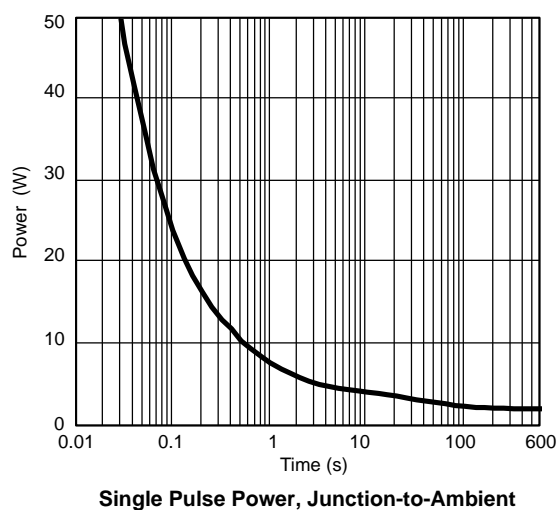
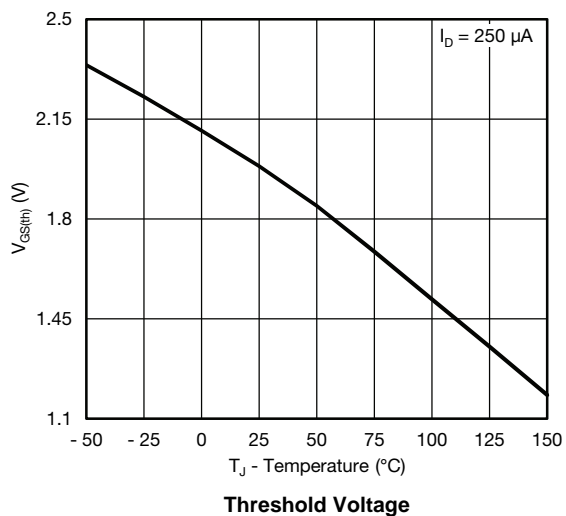
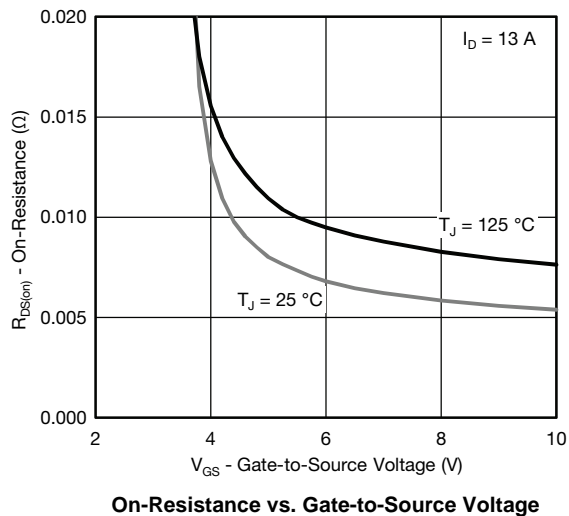
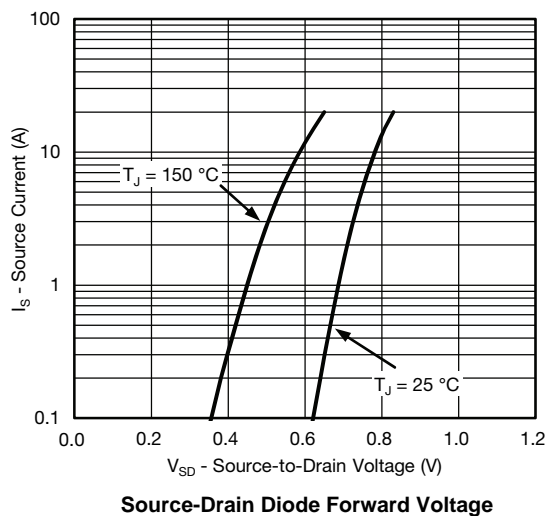
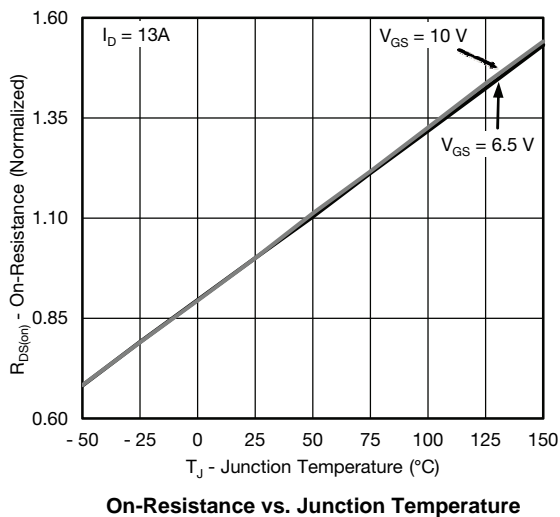
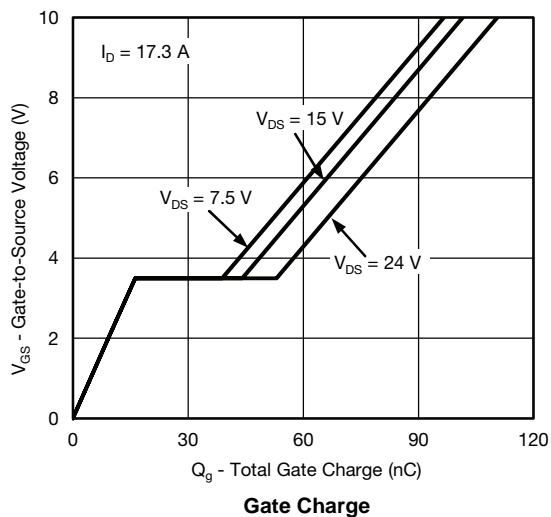


**On-Resistance vs. Drain Current**

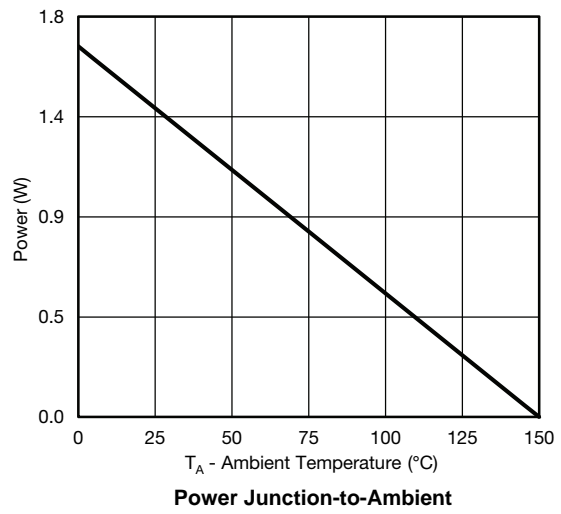
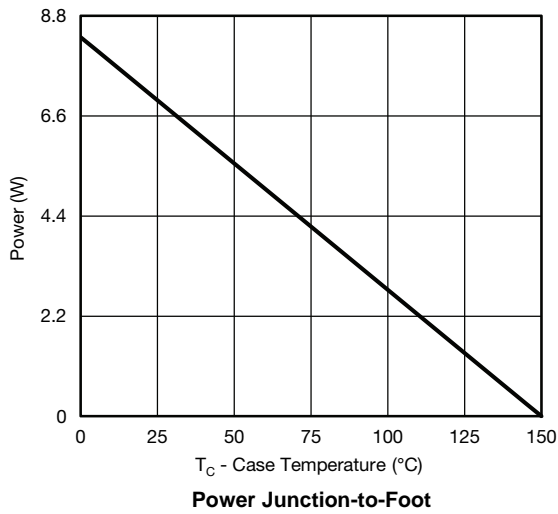
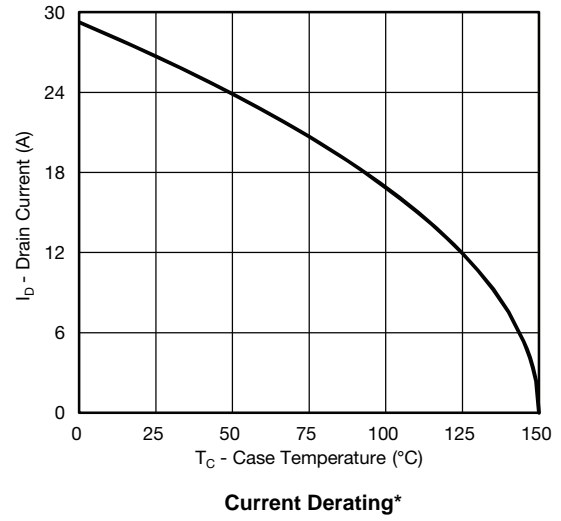
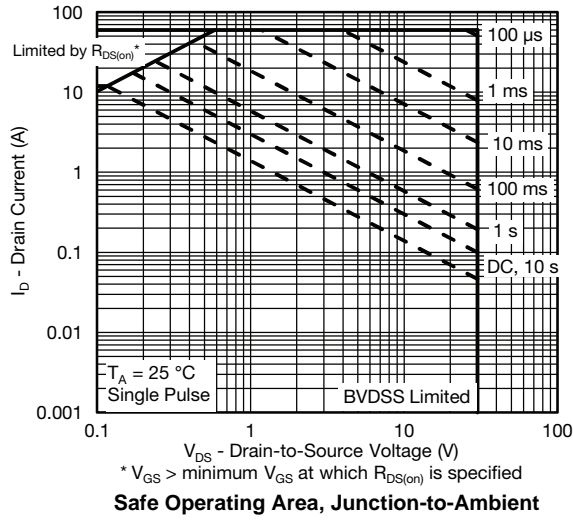


**Capacitance**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

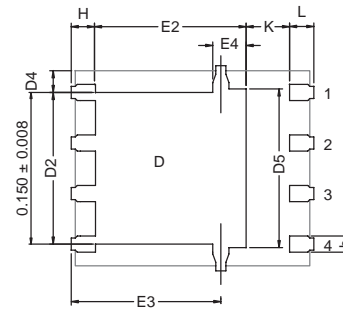
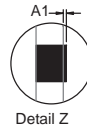
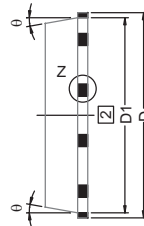
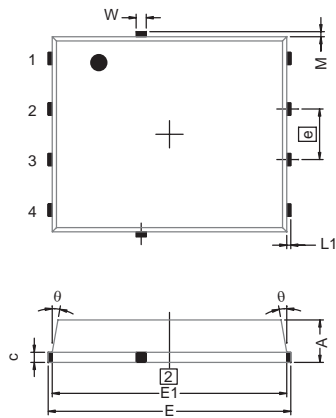


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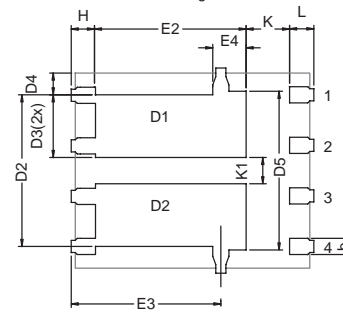


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ }^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**PowerPAK SO-8, (SINGLE/DUAL)**



Backside View of Single Pad



Backside View of Dual Pad

**Notes**

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 TYP.			0.0225 TYP.		
D5	3.98 TYP.			0.157 TYP.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 TYP.			0.030 TYP.		
Ⓜ	1.27 BSC			0.050 BSC		
K	1.27 TYP.			0.050 TYP.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		
ECN: T10-0055-Rev. J, 15-Feb-10						
DWG: 5881						

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