

# VSB003N02MS-VB Datasheet N-Channel 30 V (D-S) MOSFET

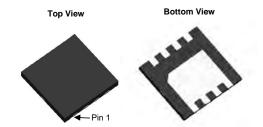
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
30	0.0018 at $V_{GS} = 10 \text{ V}$	70	22.5 nC		
30	0.0025 at V <sub>GS</sub> = 4.5 V	60	22.3110		

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 **Definition**
- Trench Gen IV Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



#### DFN 3x3 EP

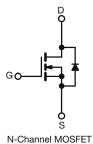


#### **APPLICATIONS**

- Switch Mode Power Supplies
- Personal Computers and Servers
- Telecom Bricks
- VRM's and POL

#### Top View





ABSOLUTE MAXIMUM RATIN	IGS (1A - 23 C			1	
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		$V_{DS}$	30	V	
Gate-Source Voltage		V <sub>GS</sub>	+ 20, - 16	v	
	T <sub>C</sub> = 25 °C		70		
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 70 °C		50		
Continuous Drain Current (1) = 190 C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	30.9 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		28.3 <sup>a, b</sup>	Α	
Pulsed Drain Current (t = 300 μs)		I <sub>DM</sub>	80		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	1-	40 <sup>g</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	3.3 <sup>a, b</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20		
Single Pulse Avalanche Energy	L=0.11IIII	E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		52		
Maximum Dawar Dissination	T <sub>C</sub> = 70 °C	ь	43	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.7 <sup>a, b</sup>	VV	
	T <sub>A</sub> = 70 °C		3.1 <sup>a, b</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature)		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, e</sup>	t ≤ 10 s	R <sub>thJA</sub>	24	33	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.9	2.4	O/ <b>VV</b>	

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. The DFN 3 x 3 is a leadless package. The end of the lead terminal is exposed pper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components. e. Maximum under steady state conditions is 81 °C/W.
- f. Based on  $T_C = 25$  °C. g. Package limited.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	<u>.                                      </u>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	/т.		14		m\//00	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_{D} = 250 \mu A$		- 5.5		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.1		2.2	٧	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ V}, -16 \text{ V}$			± 100	nA	
Zava Cata Valta na Duain Courset	1	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	,	
Zero Gate Voltage Drain Current	Itage Drain Current $I_{DSS}$ $V_{DS} = 30 \text{ V, } V_{GS} = 0 \text{ V, } T_J = 55 \text{ C}$				10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
Drain Course On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0018		Ω	
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.0025			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		105		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			3050		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1040			
Reverse Transfer Capacitance	C <sub>rss</sub>	$v_{DS} = 15 \text{ v}, v_{GS} = 0 \text{ v}, 1 = 1 \text{ MHz}$		79			
C <sub>rss</sub> /C <sub>iss</sub> Ratio				0.022	0.044		
Total Cata Charma	Q <sub>g</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		51	77	nC	
Total Gate Charge				22.5	34		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		8.6			
Gate-Drain Charge	$Q_{gd}$			4			
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V		30.5			
Gate Resistance	$R_g$	f = 1 MHz	0.3	1.25	2.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			24	48		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		17	34		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ 10 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		25	50		
Fall Time	t <sub>f</sub>			10	20		
Turn-On Delay Time	t <sub>d(on)</sub>			12	24	- ns -	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		30	60	1	
Fall Time	t <sub>f</sub>			8	16	1	
Drain-Source Body Diode Characteristic	cs		•				
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C			40	_	
Pulse Diode Forward Current	I <sub>SM</sub>				80	A	
Body Diode Voltage	V <sub>SD</sub>	$I_S = 5 A, V_{GS} = 0 V$		0.73	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			36	70	ns	
Body Diode Reverse Recovery Charge		L 10 A dl/dt _ 100 A/vo T _ 05 °C		24	48	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		16			
Reverse Recovery Rise Time	t <sub>b</sub>	7		20		ns	

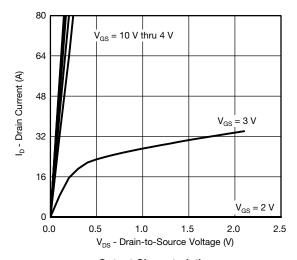
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 % b. Guaranteed by design, not subject to production testing.

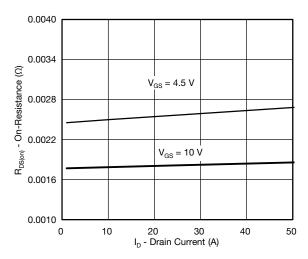
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



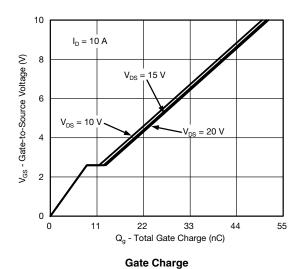
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

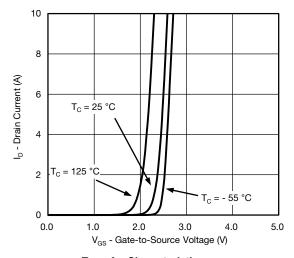


#### **Output Characteristics**

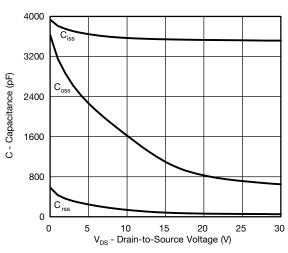


On-Resistance vs. Drain Current and Gate Voltage

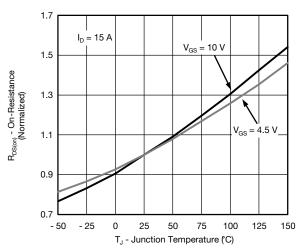




**Transfer Characteristics** 



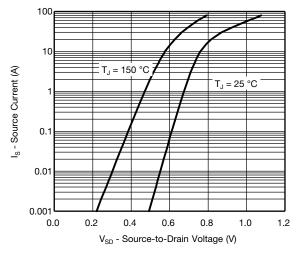
Capacitance



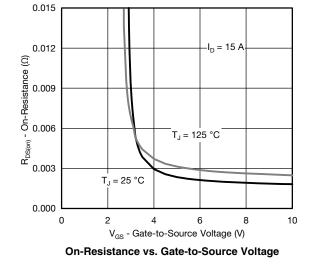
On-Resistance vs. Junction Temperature

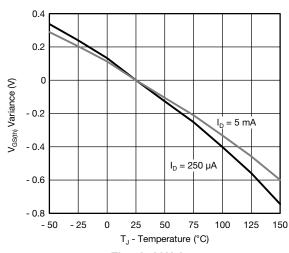


### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

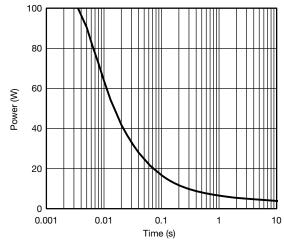


#### Source-Drain Diode Forward Voltage

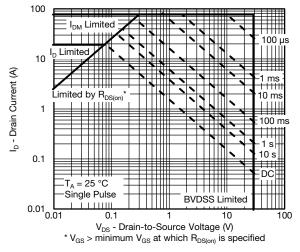




**Threshold Voltage** 



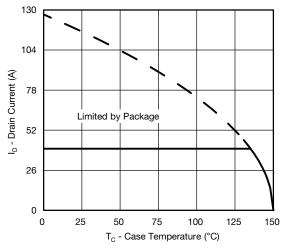
Single Pulse Power, Junction-to-Ambient



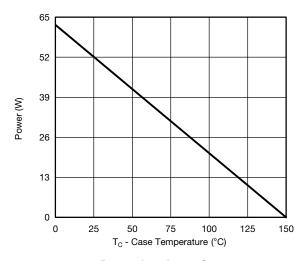
Safe Operating Area, Junction-to-Ambient

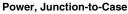


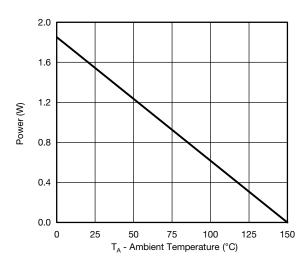
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### **Current Derating\***







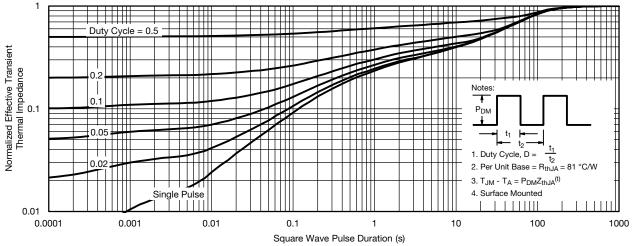
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

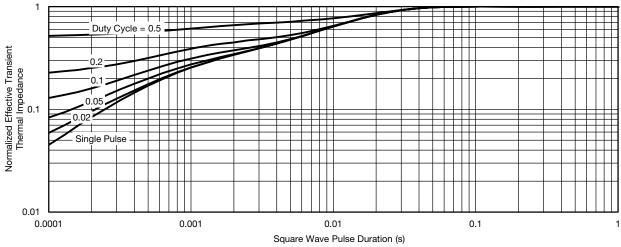
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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

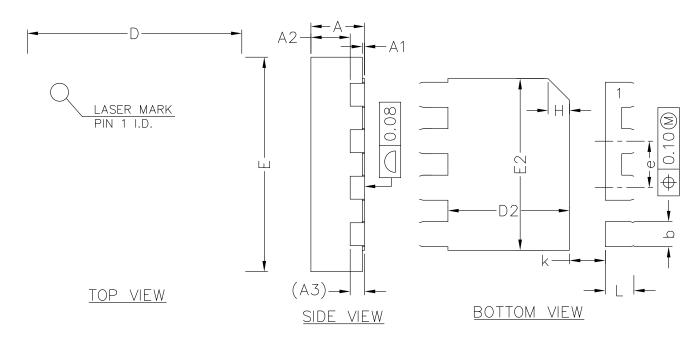


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX		
Α	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.50	0.55	0.60		
A3	0.20REF				
b	0.30	0.35	0.40		
D	2.90	3.00	3.10		
E	2.90	3.00	3.10		
D2	1.60	1.70	1.80		
E2	2.30	2.40	2.50		
е	0.55	0.65	0.75		
K	0.40	0.50	0.60		
L	0.35	0.40	0.45		



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