

Si7117DN-VB Datasheet

P-Channel 200V (D-S)MOSFET

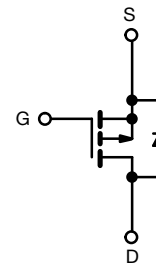
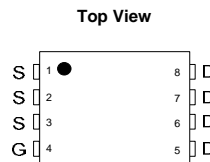
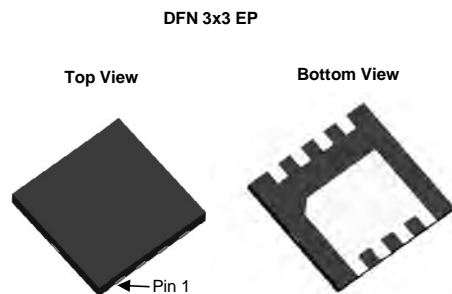
| PRODUCT SUMMARY | | |
|---------------------------|-------------------------|-----|
| V_{DS} (V) | -200 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = -10\text{ V}$ | 2.0 |
| Q_g max. (nC) | 29 | |
| Q_{gs} (nC) | 5.4 | |
| Q_{gd} (nC) | 15 | |
| Configuration | Single | |

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling



RoHS*
Available
HALOGEN
FREE
Available



P-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | | |
|---|--------------------------|-------------------------|-----------------------------------|-------------|------|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | | V _{DS} | -200 | V |
| Gate-Source Voltage | | | V _{GS} | ± 20 | |
| Continuous Drain Current | V _{GS} at -10 V | T _C = 25 °C | I _D | -3.6 | A |
| | | T _C = 100 °C | | -2.5 | |
| Pulsed Drain Current ^a | | | I _{DM} | -12 | W/°C |
| Linear Derating Factor | | | | 0.59 | |
| Linear Derating Factor (PCB mount) ^e | | | | 0.025 | |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 500 | mJ |
| Avalanche Current ^a | | | I _{AR} | -6.4 | A |
| Repetitive Avalanche Energy ^a | | | E _{AR} | 7.4 | mJ |
| Maximum Power Dissipation | T _C = 25 °C | | P _D | 74 | W |
| Maximum Power Dissipation (PCB mount) ^e | T _A = 25 °C | | | 3.0 | |
| Peak Diode Recovery dV/dt ^c | | | dV/dt | -5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | -55 to +150 | °C |
| Soldering Recommendations (Peak temperature) ^d | for 10 s | | | 300 | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 17\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = -6.5\text{ A}$ (see fig. 12).
- $I_{SD} \leq -6.5\text{ A}$, $dI/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

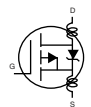

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|--|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB mount) ^a | R_{thJA} | - | 40 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.7 | |

Note

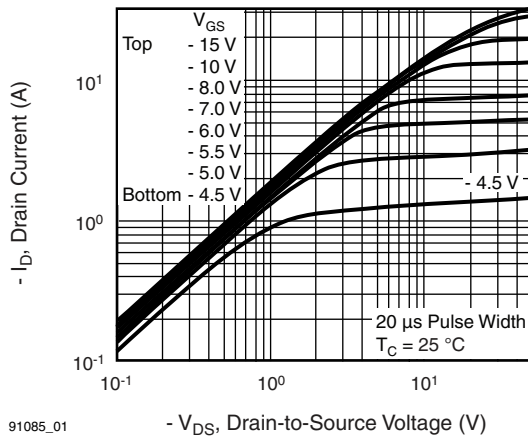
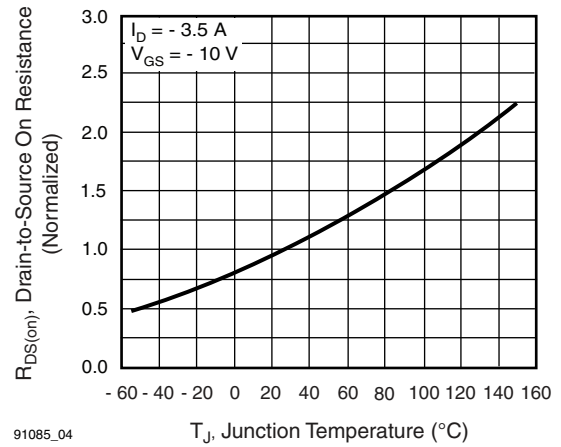
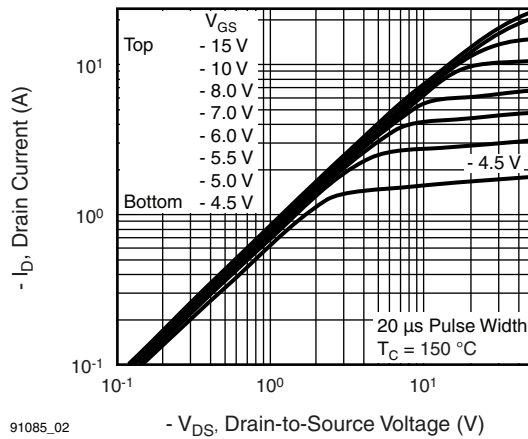
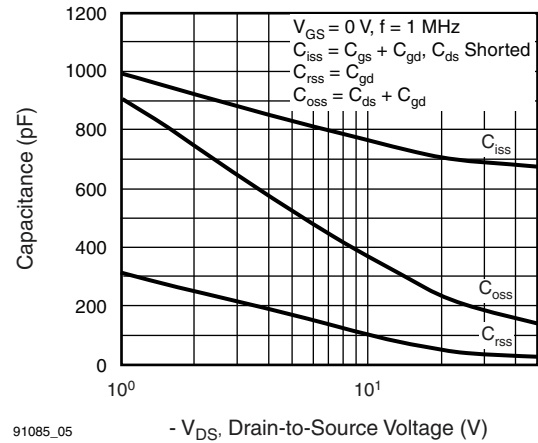
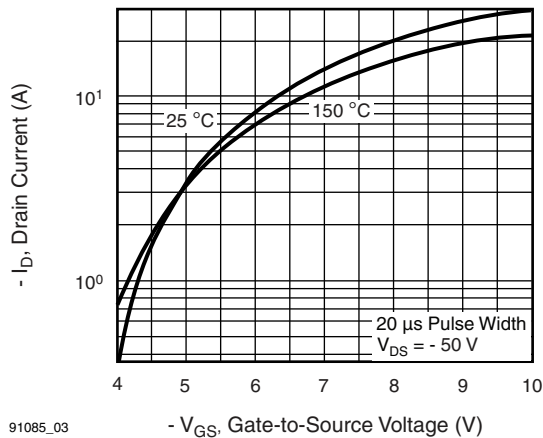
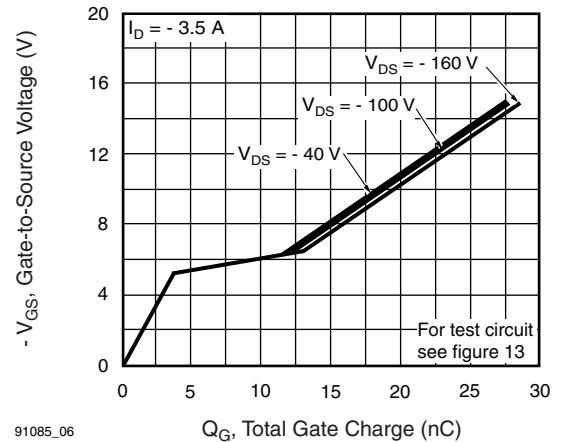
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---------------------|--|------|-------|----------|-----------------------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0$, $I_D = -250\text{ }\mu\text{A}$ | -200 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^{\circ}\text{C}$, $I_D = -1\text{ mA}$ | - | -0.24 | - | V/ $^{\circ}\text{C}$ |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$ | -1.5 | - | -4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | - | - | ± 10 | μA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -200\text{ V}$, $V_{GS} = 0\text{ V}$ | - | - | -100 | μA |
| | | $V_{DS} = -160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$ | - | - | -500 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = -10\text{ V}$, $I_D = -1.0\text{ A}$ ^b | - | 2.00 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = -50\text{ V}$, $I_D = -1.0\text{ A}$ ^b | 2.8 | - | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 | - | 700 | - | pF |
| Output Capacitance | C_{oss} | | - | 200 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 40 | - | |
| Total Gate Charge | Q_g | $V_{GS} = -10\text{ V}$, $I_D = -3.5\text{ A}$, $V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b | - | - | 29 | nC |
| Gate-Source Charge | Q_{gs} | | - | - | 5.4 | |
| Gate-Drain Charge | Q_{gd} | | - | - | 15 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -100\text{ V}$, $I_D = -3.5\text{ A}$, $R_g = 12\text{ }\Omega$, $R_D = 15\text{ }\Omega$, see fig. 10 ^b | - | 12 | - | ns |
| Rise Time | t_r | | - | 27 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 28 | - | |
| Fall Time | t_f | | - | 24 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | - | 7.5 | - | |
| Gate Input Resistance | R_g | $f = 1\text{ MHz}$, open drain | 0.6 | - | 3.7 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | -3.5 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | -6 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_S = -3.5\text{ A}$, $V_{GS} = 0\text{ V}$ ^b | - | - | -6.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_F = -3.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$ ^b | - | 200 | 300 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 1.9 | 2.9 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

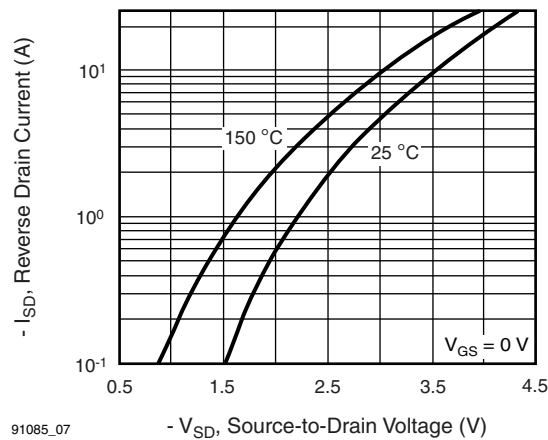


Fig. 7 - Typical Source-Drain Diode Forward Voltage

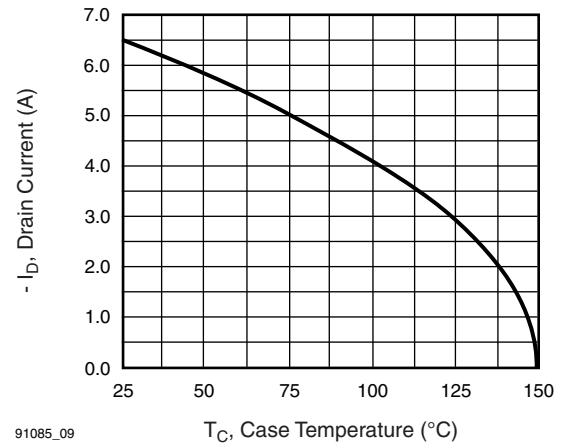


Fig. 9 - Maximum Drain Current vs. Case Temperature

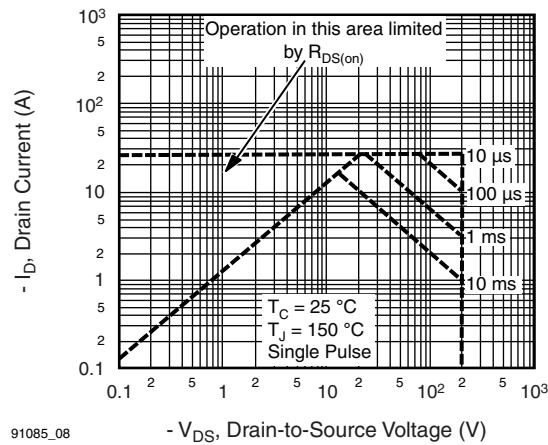


Fig. 8 - Maximum Safe Operating Area

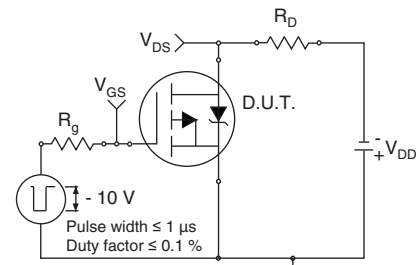


Fig. 10a - Switching Time Test Circuit

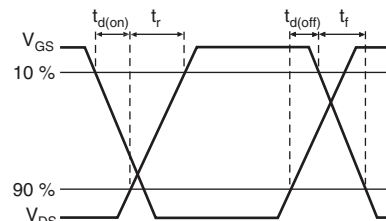


Fig. 10b - Switching Time Waveforms

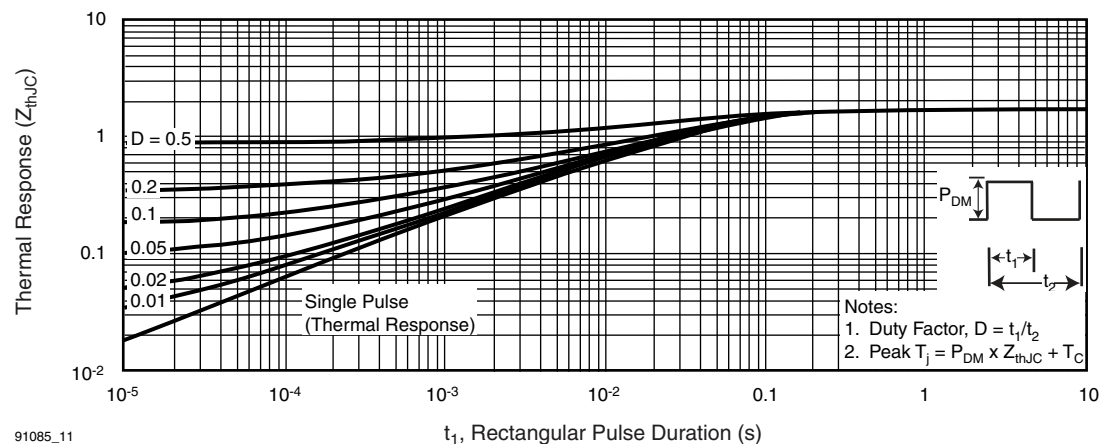


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

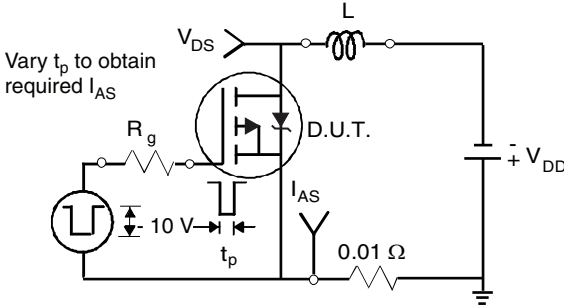


Fig. 12a - Unclamped Inductive Test Circuit

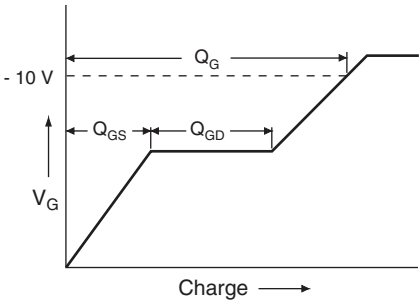


Fig. 13a - Basic Gate Charge Waveform

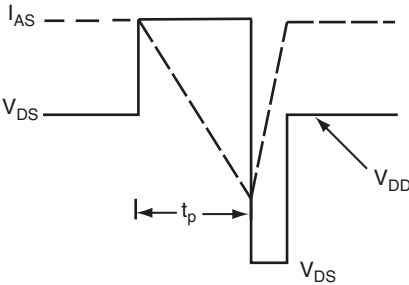


Fig. 12b - Unclamped Inductive Waveforms

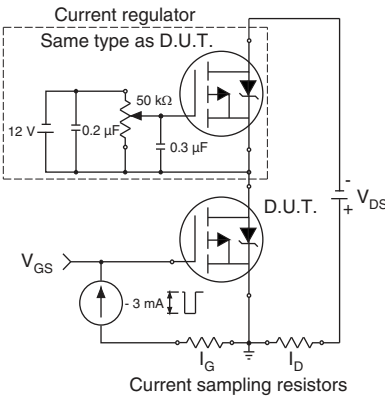


Fig. 13b - Gate Charge Test Circuit

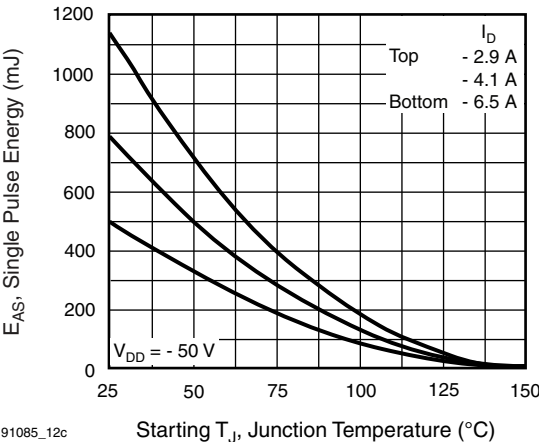
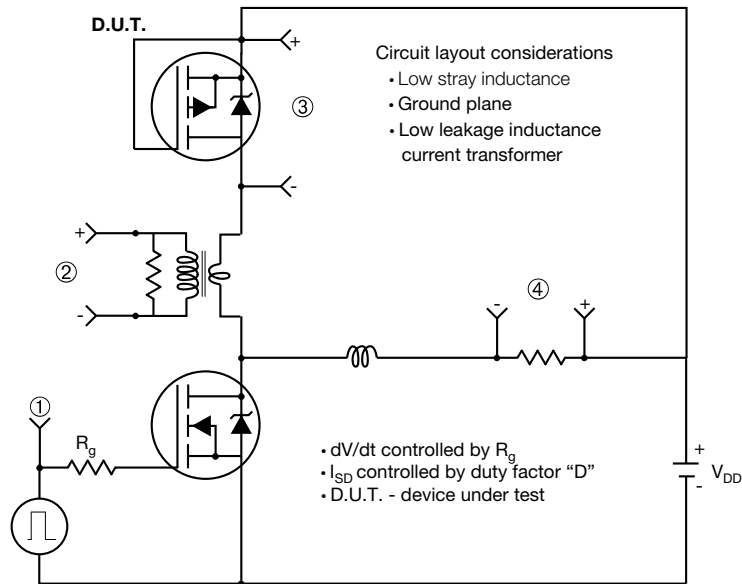


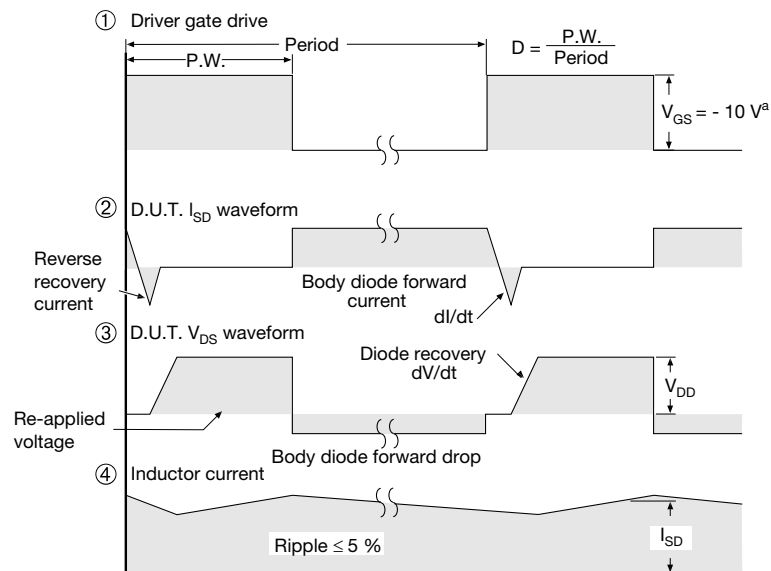
Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Peak Diode Recovery dV/dt Test Circuit



Note

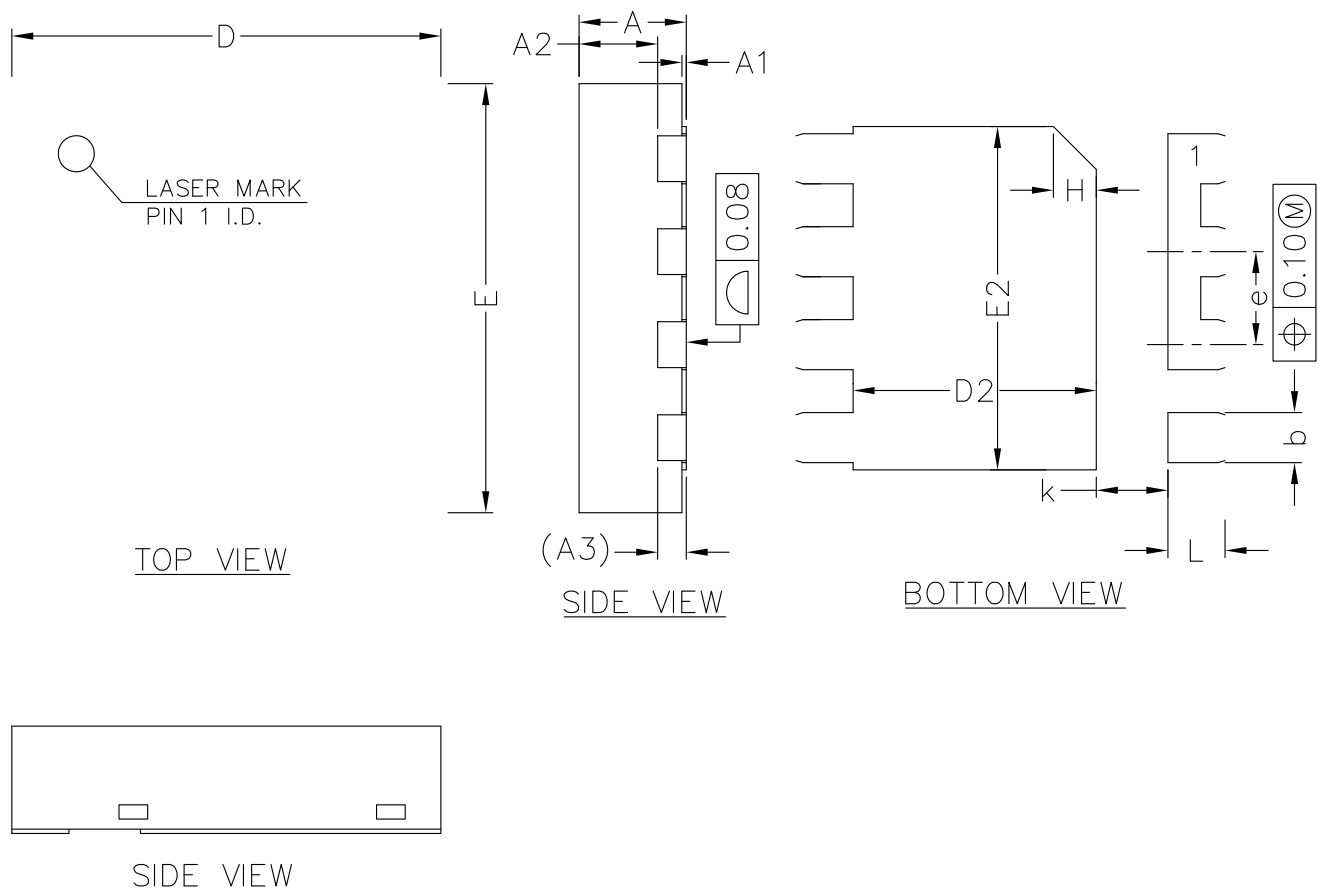
- Complement N-Channel of D.U.T. for driver



Note

a. $V_{GS} = -5 V$ for logic level and $-3 V$ drive devices

Fig. 14 - For P-Channel



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|--------|---------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | 0.50 | 0.55 | 0.60 |
| A3 | 0.20REF | | |
| b | 0.30 | 0.35 | 0.40 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| D2 | 1.60 | 1.70 | 1.80 |
| E2 | 2.30 | 2.40 | 2.50 |
| e | 0.55 | 0.65 | 0.75 |
| K | 0.40 | 0.50 | 0.60 |
| L | 0.35 | 0.40 | 0.45 |

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