

STL9P3LLH6-VB Datasheet

P-Channel 30 V (D-S) MOSFET

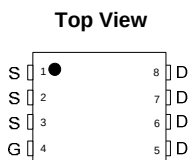
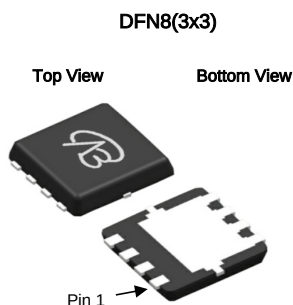
V_{DS}		-30	V
$R_{DS(on),typ}$	$V_{GS}=10V$	11	$m\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	18	$m\Omega$
I_D		-45	A

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- Low Thermal Resistance Power Package with Small Size and Low 1.07 mm Profile
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

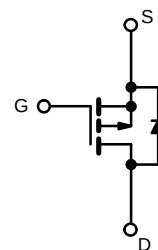


RoHS
COMPLIANT
HALOGEN
FREE



APPLICATIONS

- Load Switch
- Adaptor Switch
- Notebook PC



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150\text{ }^\circ\text{C}$)	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 70\text{ }^\circ\text{C}$	
		$T_A = 25\text{ }^\circ\text{C}$	
		$T_A = 70\text{ }^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	- 60	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	
		$T_A = 25\text{ }^\circ\text{C}$	
Avalanche Current	I_{AS}	- 25	mJ
Single-Pulse Avalanche Energy	E_{AS}	31.25	
Maximum Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
		$T_C = 70\text{ }^\circ\text{C}$	
		$T_A = 25\text{ }^\circ\text{C}$	
		$T_A = 70\text{ }^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 50 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. $t = 10\text{ s}$.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

d. Package limited.

e. Based on $T_C = 25\text{ }^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	26	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 81 °C/W.

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 20		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.5		- 2.8	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 14.4 A		11		mΩ
		V _{GS} = - 4.5 V, I _D = - 11.5 A		18		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 14.4 A		37		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		2000		pF
Output Capacitance	C _{oss}			385		
Reverse Transfer Capacitance	C _{rss}			322		
Total Gate Charge	Q _g	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 14.4 A			15	nC
					14	
Gate-Source Charge	Q _{gs}	V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 14.4 A			7	
Gate-Drain Charge	Q _{gd}				9	
Gate Resistance	R _g	f = 1 MHz	0.4	1.8	3.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.5 Ω I _D ≡ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		50	75	ns
Rise Time	t _r			43	65	
Turn-Off DelayTime	t _{d(off)}			30	45	
Fall Time	t _f			14	21	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.5 Ω I _D ≡ - 10 A, V _{GEN} = - 10 V, R _g = 1 Ω		14	21	
Rise Time	t _r			9	18	
Turn-Off DelayTime	t _{d(off)}			36	54	
Fall Time	t _f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 35 ^e	A
Pulse Diode Forward Current ^a	I _{SM}				- 60	
Body Diode Voltage	V _{SD}	I _F = - 10 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10 A, di/dt = 100 A/μs, T _J = 25 °C		31	47	ns
Body Diode Reverse Recovery Charge	Q _{rr}			30	45	nC
Reverse Recovery Fall Time	t _a			15		ns
Reverse Recovery Rise Time	t _b			16		

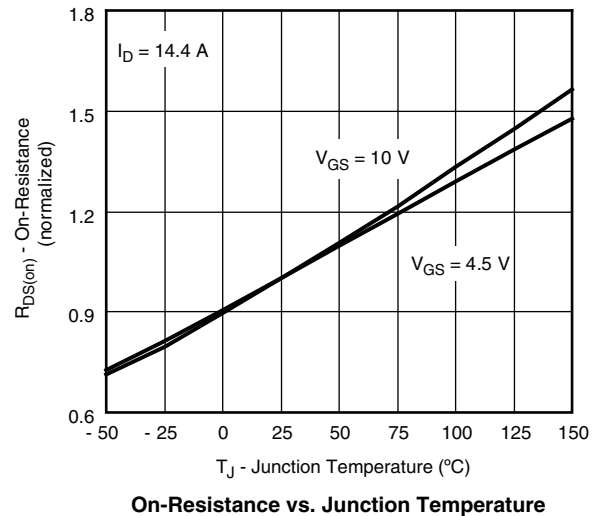
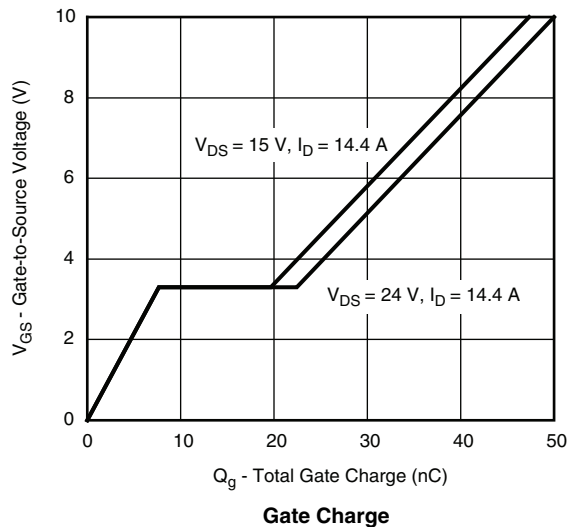
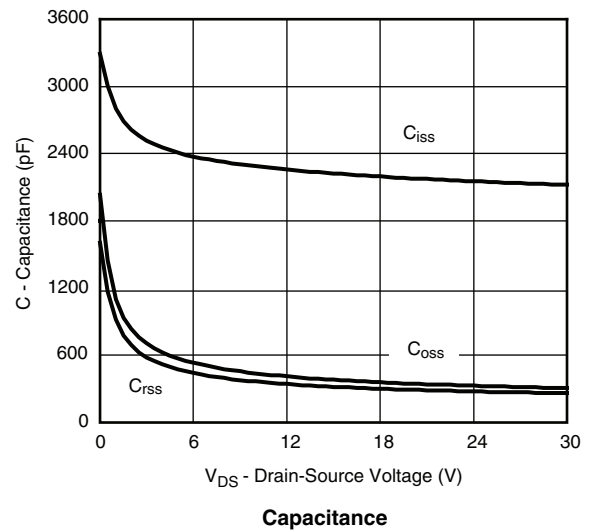
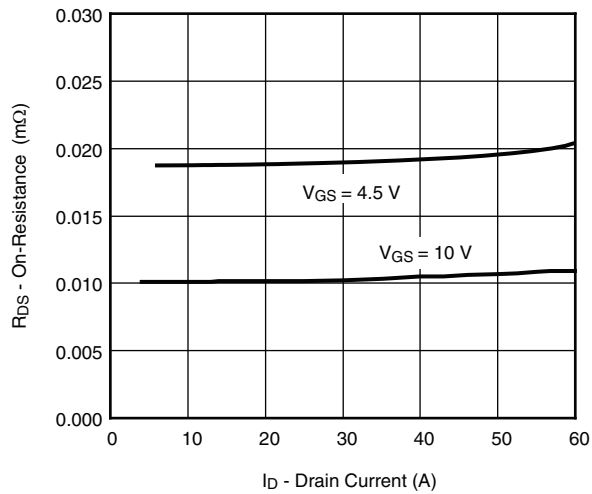
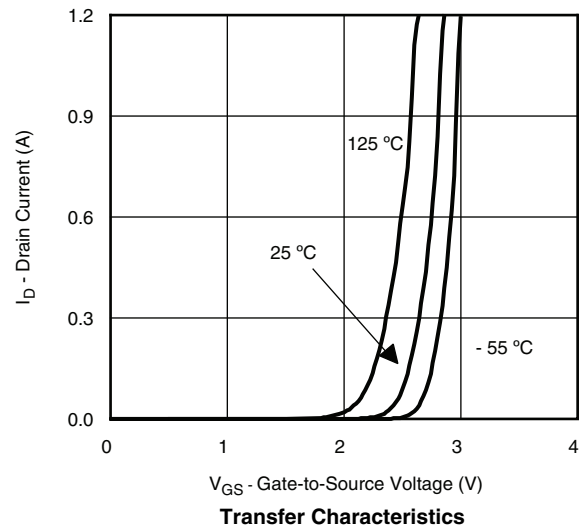
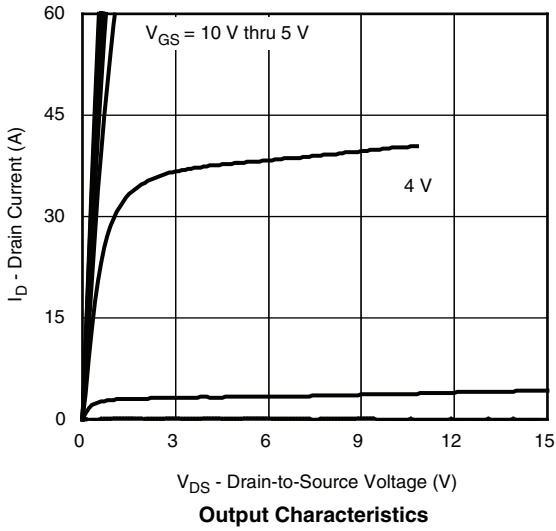
Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

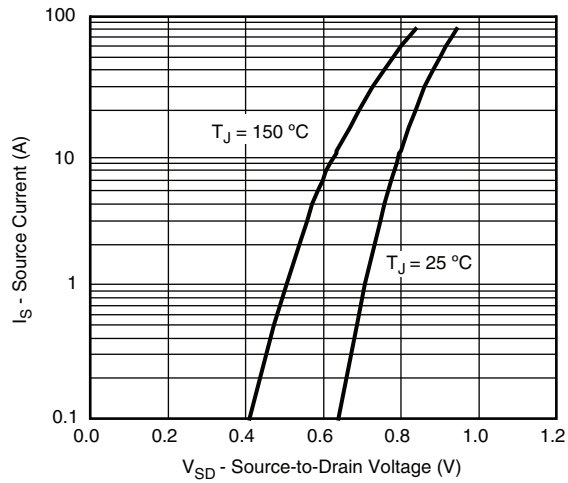
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

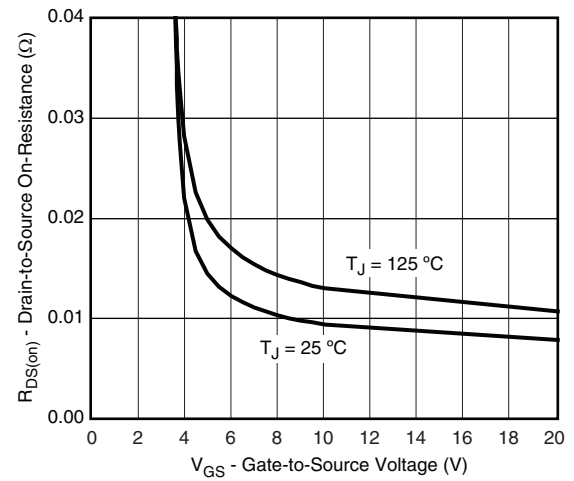
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



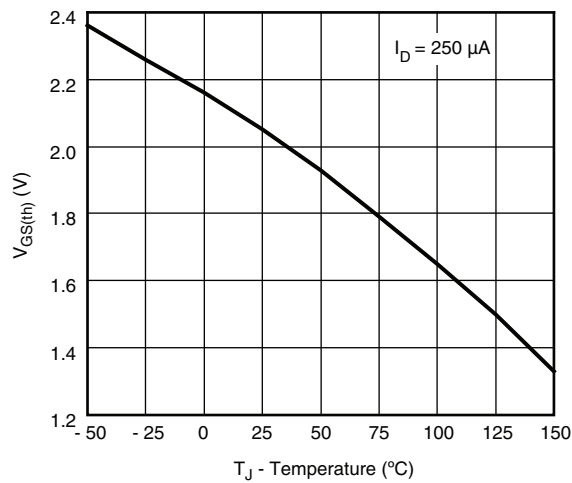
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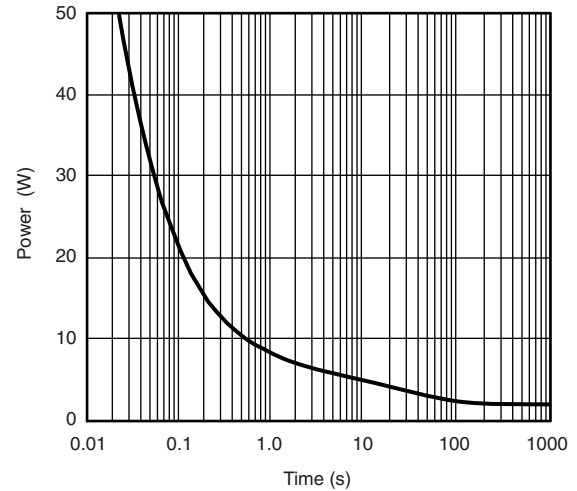
Source-Drain Diode Forward Voltage



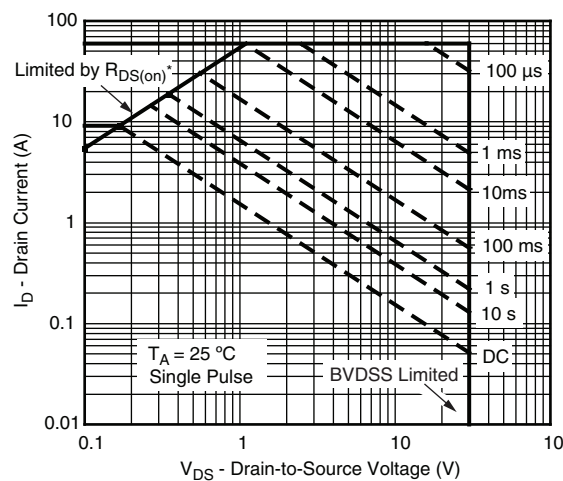
On-Resistance vs. Gate-to-Source Voltage



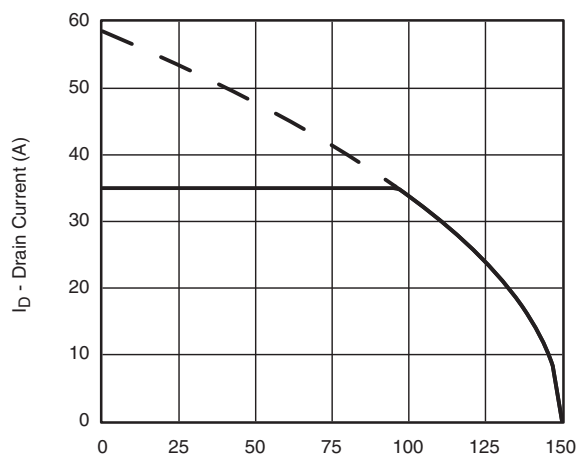
Threshold Voltage



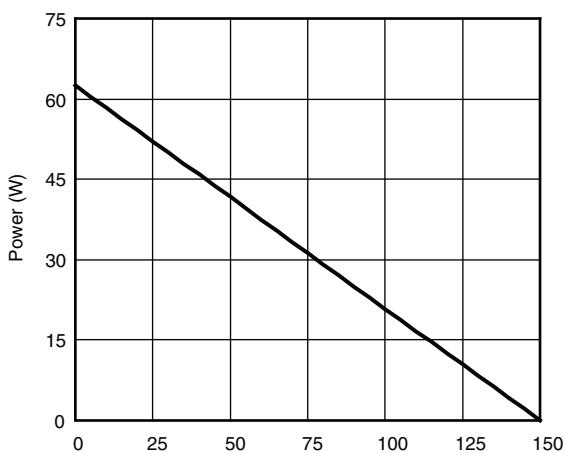
Single Pulse Power, Junction-to-Ambient



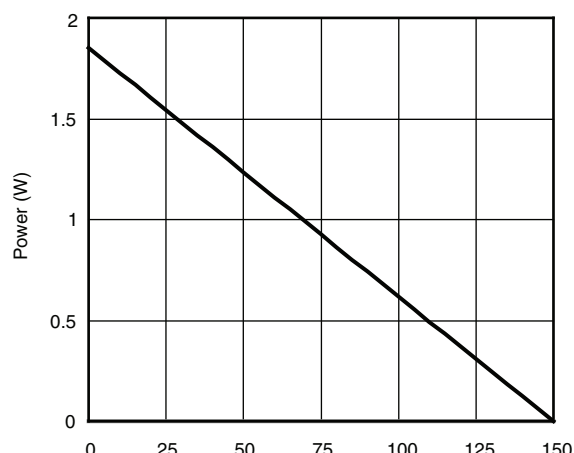
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


T_C - Case Temperature (°C)
Current Derating*



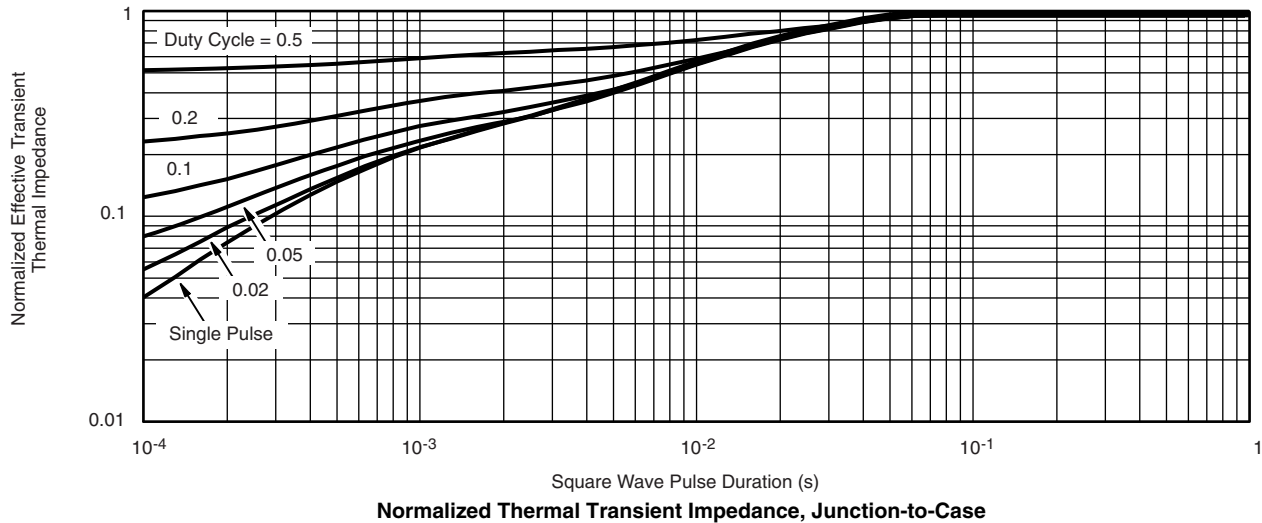
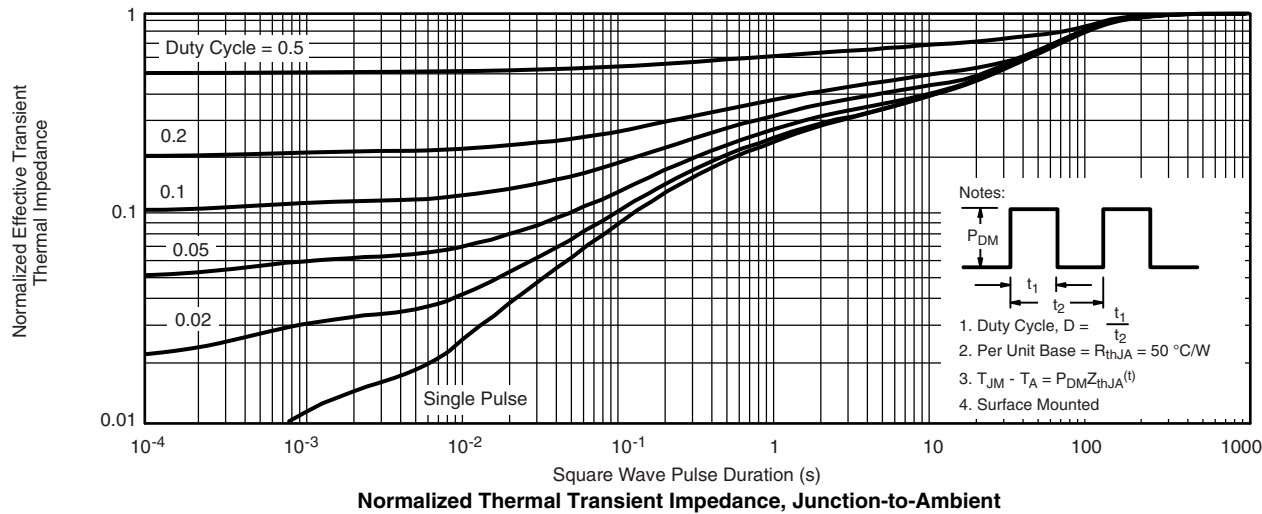
T_C - Case Temperature (°C)
Power, Junction-to-Case



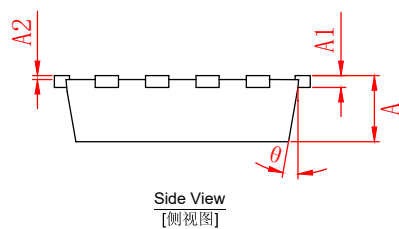
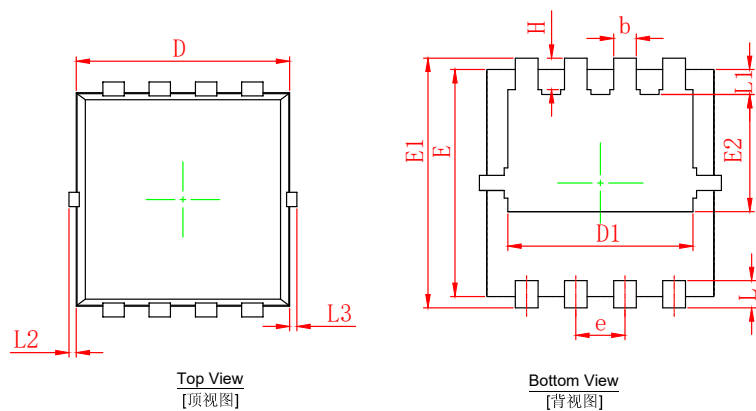
T_A - Ambient Temperature (°C)
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

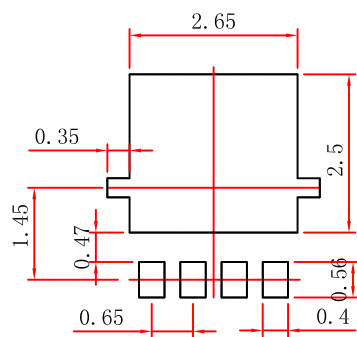


PDFNWB3×3-8L Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



- Note:
- 1.Controlling dimension:in millimeters.
 - 2.General tolerance:±0.05mm.
 - 3.The pad layout is for reference purposes only.

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