N7458-VB Datasheet

N-Channel 250 V (D-S) MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	250
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.125
$R_{DS(on)}$ (Ω) at V_{GS} = 7.5 V	0.135
Q_g typ. (nC)	8.6
I_D (A)	10.3 [f]
Configuration	Single

FEATURES

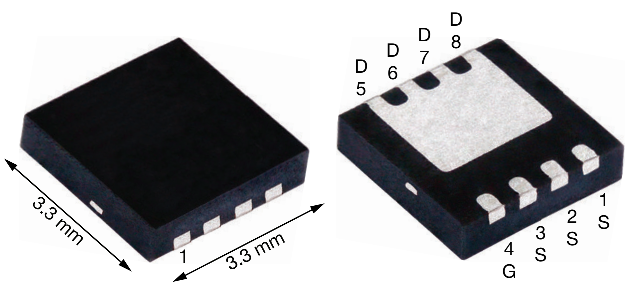
- Trench power MOSFET
- Low thermal resistance package
- 100 % R_g and UIS tested

RoHS COMPLIANT
HALOGEN FREE

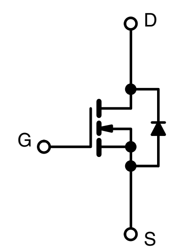
APPLICATIONS

- Primary side switch
- Synchronous rectification
- DC/DC converter
- Lighting
- Industrial

DFN 3x3 EP



Top View   Bottom View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	250	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	10.3	A
	T_C = 70 °C		6.8	
	T_A = 25 °C		3.7 [a, b]	
	T_A = 70 °C		3 [a, b]	
Pulsed drain current (t = 100 μs)		I_{DM}	25	
Continuous source-drain diode current	T_C = 25 °C	I_S	45	
	T_A = 25 °C		4.2 [a, b]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	12	
Single pulse avalanche energy		E_{AS}	7.2	mJ
Maximum power dissipation	T_C = 25 °C	P_D	24.2	W
	T_C = 70 °C		14.8	
	T_A = 25 °C		3.5 [a, b]	
	T_A = 70 °C		2.2 [a, b]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [a]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a]	t ≤ 10 s	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.8	2.3	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. t = 10 s

c. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

e. Maximum under steady state conditions is 65 °C/W

f. T_C = 25 °C

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	250	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	-	254	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-6.9	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	2	-	4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 250 V, V_{GS} = 0 V, T_J = 70 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} =10 V	10	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} =10 V, I_D = 3.7 A	-	0.125	-	Ω
		V_{GS} = 7.5 V, I_D = 3.5 A	-	0.135	-	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 3.7 A	-	10	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 125 V, V_{GS} = 0 V, f = 1 MHz	-	600	-	pF
Output capacitance	C_{oss}		-	65	-	
Reverse transfer capacitance	C_{rss}		-	2	-	
Total gate charge	Q_g	V_{DS} = 125 V, V_{GS} = 10 V, I_D = 2 A	-	10.9	16.5	nC
		V_{DS} = 125 V, V_{GS} = 7.5 V, I_D = 2 A	-	8.6	12.9	
Gate-source charge	Q_{gs}		-	2.7	-	
Gate-drain charge	Q_{gd}		-	2.9	-	
Output charge	Q_{oss}	V_{DS} = 125 V, V_{GS} = 0 V	-	30	45	
Gate resistance	R_g	f = 1 MHz	0.5	2.3	4.6	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 125 V, R_L = 41.7 Ω, $I_D \cong$ 3 A, V_{GEN} = 10 V, R_g = 1 Ω	-	8	16	ns
Rise time	t_r		-	22	35	
Turn-off delay time	$t_{d(off)}$		-	18	30	
Fall time	t_f		-	22	35	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 125 V, R_L = 41.7 Ω, $I_D \cong$ 3 A, V_{GEN} = 7.5 V, R_g = 1 Ω	-	10	20	
Rise time	t_r		-	22	40	
Turn-off delay time	$t_{d(off)}$		-	18	30	
Fall time	t_f		-	25	50	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	45	A
Pulse diode forward current	I_{SM}		-	-	25	
Body diode voltage	V_{SD}	I_S = 3.4 A, V_{GS} = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 3.4 A, di/dt = 100 A/μs, T_J = 25 °C	-	100	150	ns
Body diode reverse recovery charge	Q_{rr}		-	356	550	nC
Reverse recovery fall time	t_a		-	65	-	ns
Reverse recovery rise time	t_b		-	35	-	

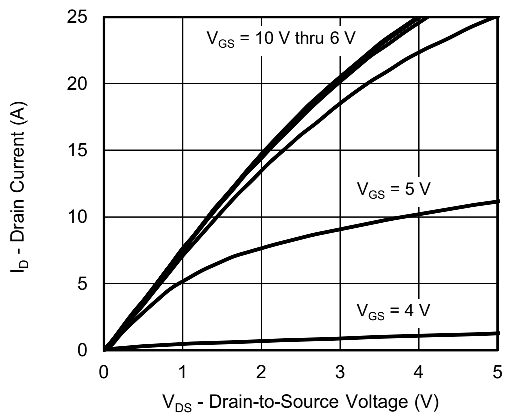
Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

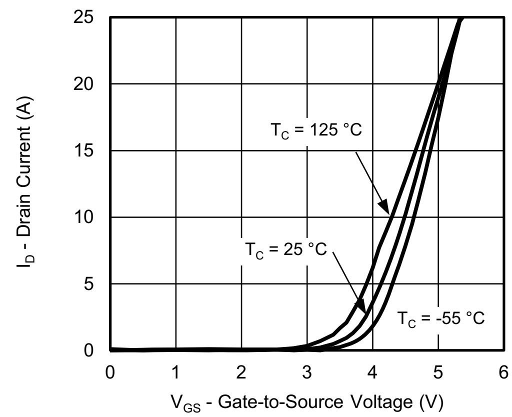
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

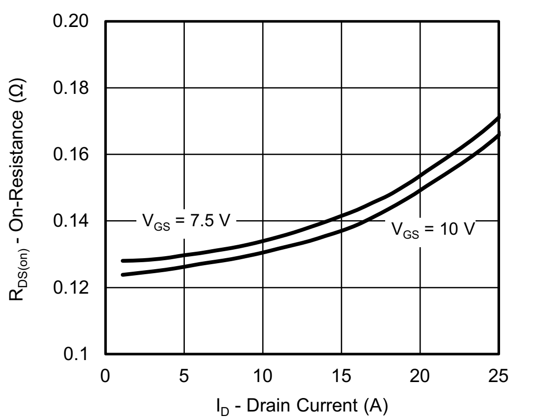
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



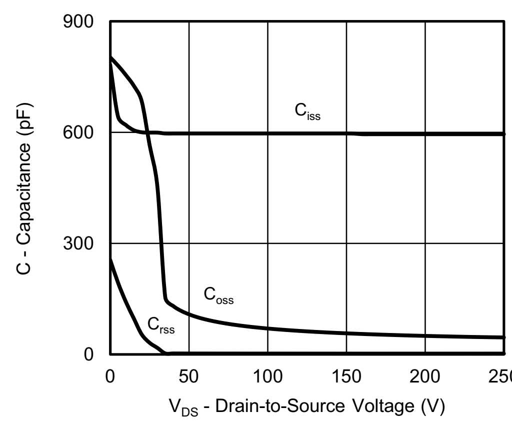
Output Characteristics



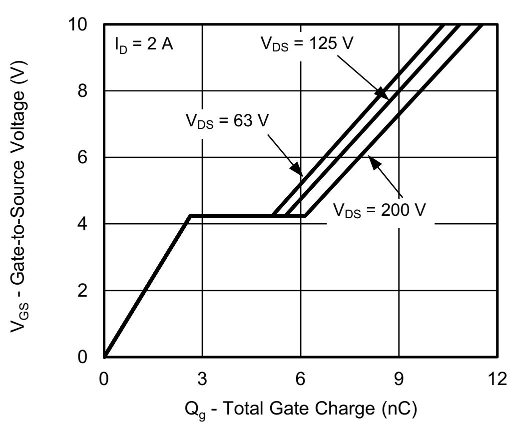
Transfer Characteristics



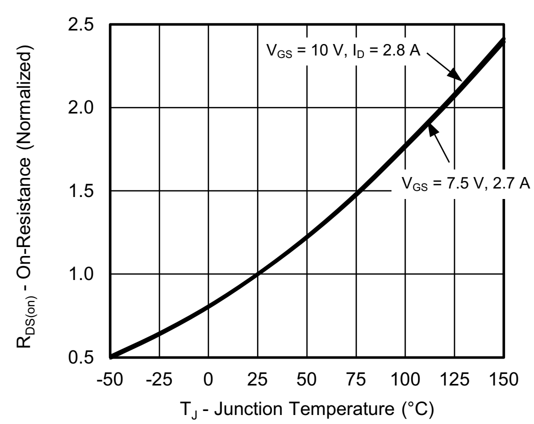
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

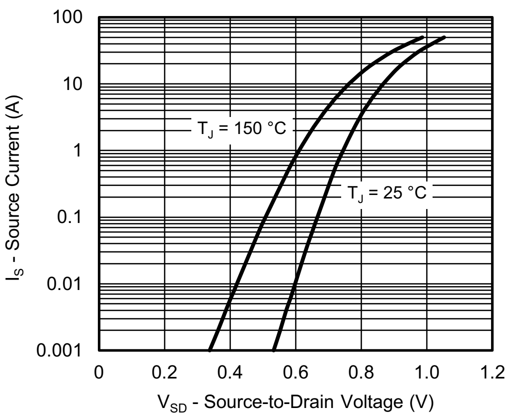


Gate Charge

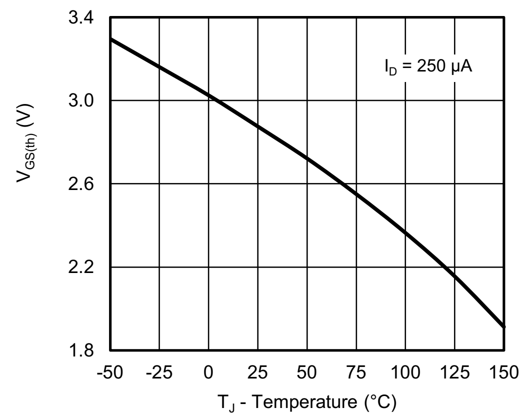


On-Resistance vs. Junction Temperature

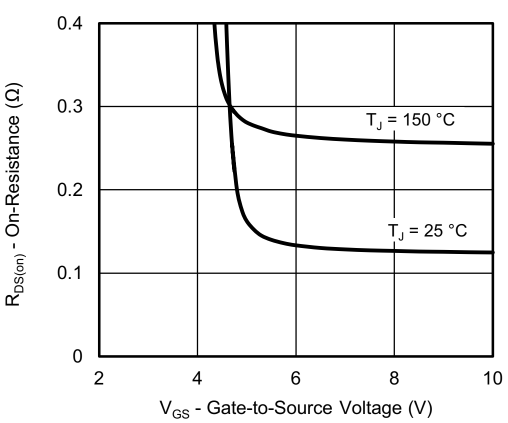
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



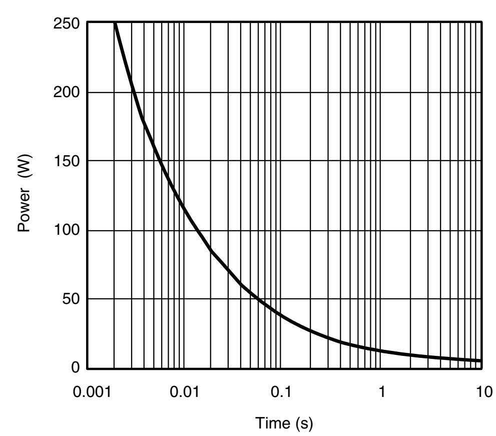
Source-Drain Diode Forward Voltage



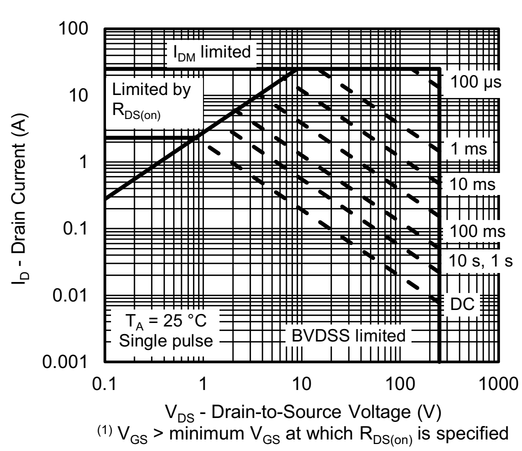
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

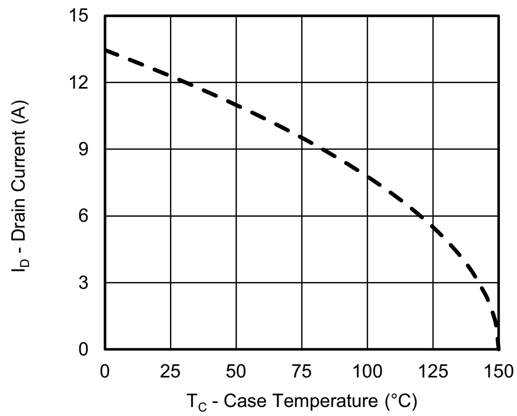


Single Pulse Power, Junction-to-Ambient

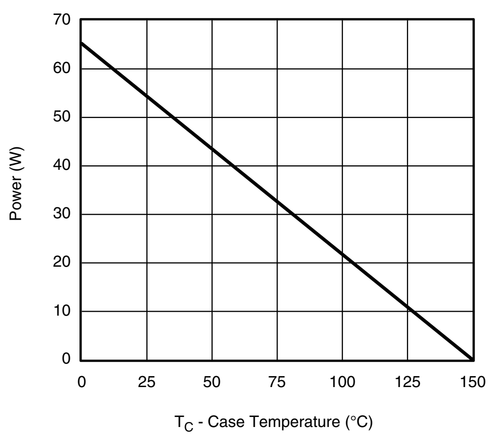


Safe Operating Area, Junction-to-Ambient

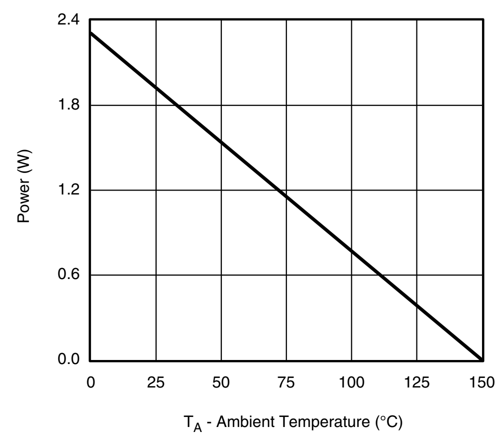
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

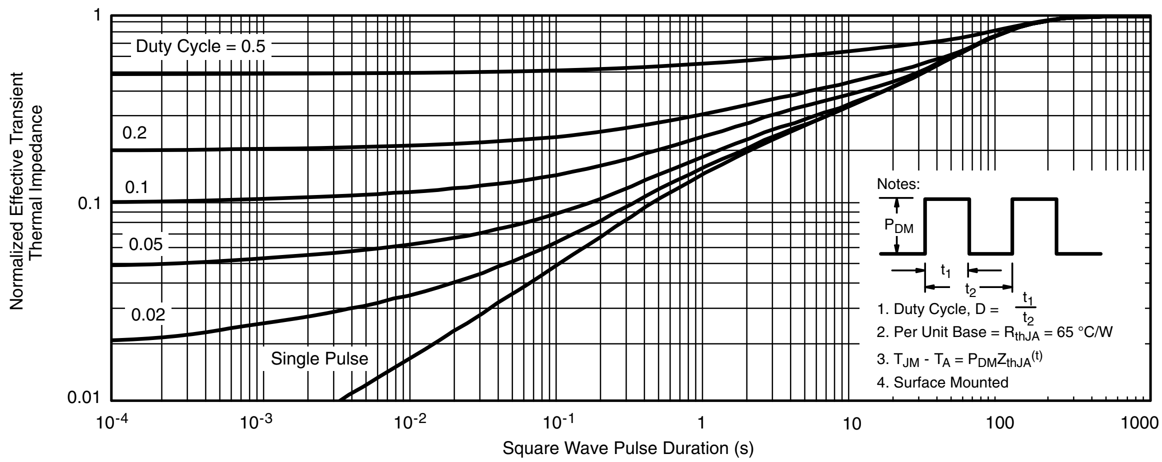


Power, Junction-to-Ambient

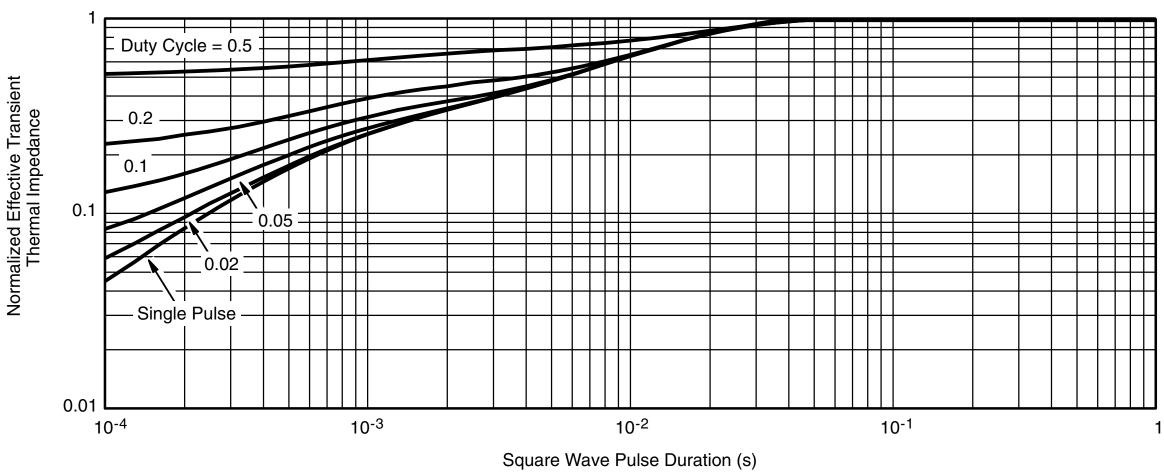
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

Taiwan VBsemi Electronics Co., Ltd., branches, agents, employees, and all persons acting on its or their representatives (collectively, the "Taiwan VBsemi"), assumes no responsibility for any errors, inaccuracies or incomplete data contained in the table or any other any disclosure of any information related to the product.(www.VBsemi.com)

Taiwan VBsemi makes no guarantee, representation or warranty on the product for any particular purpose of any goods or continuous production. To the maximum extent permitted by applicable law on Taiwan VBsemi relinquished: (1) any application and all liability arising out of or use of any products; (2) any and all liability, including but not limited to special, consequential damages or incidental ; (3) any and all implied warranties, including a particular purpose, non-infringement and merchantability guarantee.

Statement on certain types of applications are based on knowledge of the product is often used in a typical application of the general product VBsemi Taiwan demand that the Taiwan VBsemi of. Statement on whether the product is suitable for a particular application is non-binding. It is the customer's responsibility to verify specific product features in the products described in the specification is appropriate for use in a particular application. Parameter data sheets and technical specifications can be provided may vary depending on the application and performance over time. All operating parameters, including typical parameters must be made by customer's technical experts validated for each customer application. Product specifications do not expand or modify Taiwan VBsemi purchasing terms and conditions, including but not limited to warranty herein.

Unless expressly stated in writing, Taiwan VBsemi products are not intended for use in medical, life saving, or life sustaining applications or any other application. Wherein VBsemi product failure could lead to personal injury or death, use or sale of products used in Taiwan VBsemi such applications using client did not express their own risk. Contact your authorized Taiwan VBsemi people who are related to product design applications and other terms and conditions in writing.

The information provided in this document and the company's products without a license, express or implied, by estoppel or otherwise, to any intellectual property rights granted to the VBsemi act or document. Product names and trademarks referred to herein are trademarks of their respective representatives will be all.

Material Category Policy

Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be oHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.