

RoHS

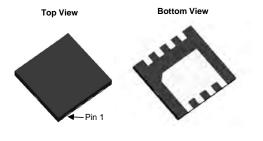
COMPLIANT HALOGEN FREE

### FDMC8015L-VB Datasheet

## N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A) <sup>f</sup>	Q <sub>g</sub> (Typ.)			
40	0.0045 at V <sub>GS</sub> = 10 V	40 <sup>g</sup>	9.8 nC			
40	0.0062 at $V_{GS}$ = 4.5 V	40 <sup>g</sup>	3.0110			

DFN 3x3 EP



#### **FEATURES**

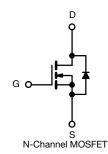
- Trench Power MOSFET
- 100 % R<sub>q</sub> and UIS Tested
- Capable of Operating with 5 V Gate Drive

#### **APPLICATIONS**

- Synchronous Rectification
- Synchronous Buck Converters
- ORing
- Load Switching
- Motor Drive Switch

#### Top View





ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage		V <sub>DS</sub>	40	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20	v		
	T <sub>C</sub> = 25 °C		40 <sup>g</sup>			
Continuous Drain Current (T 150 °C)	T <sub>C</sub> = 70 °C	- I <sub>D</sub>	40 <sup>g</sup>			
Continuous Drain Current ( $T_J = 150 \ ^{\circ}C$ )	T <sub>A</sub> = 25 °C		19.3 <sup>a, b</sup>			
	T <sub>A</sub> = 70 °C		15.5 <sup>a, b</sup>	•		
Pulsed Drain Current (t = 100 µs)		I <sub>DM</sub>	100	A		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	- I <sub>S</sub>	40 <sup>g</sup>			
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C		3.1 <sup>a, b</sup>			
Single Pulse Avalanche Current		I <sub>AS</sub>	20			
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	20	mJ		
	T <sub>C</sub> = 25 °C		52			
Movimum Dower Dissinction	T <sub>C</sub> = 70 °C		33	w		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.7 <sup>a, b</sup>	VV		
	T <sub>A</sub> = 70 °C	1	2.4 <sup>a, b</sup>			
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		
Soldering Recommendations (Peak Tempera	Ĭ	260	·U			

#### THEDMAL DESIGTANCE DATINGS

I HERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>a, e</sup>	t ≤ 10 s	R <sub>thJA</sub>	26	33	°C/W		
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.9	2.4	0/11		

#### Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s. c. The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Maximum under steady state conditions is 81 °C/W.

f. Based on  $T_C = 25$  °C. g. Package limited.

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			56		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.1		2.2	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 V$ , $V_{GS} = 10 V$	20			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0045		Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.0062			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		65		S	
Dynamic <sup>b</sup>						1	
Input Capacitance	C <sub>iss</sub>			1330		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1200			
Reverse Transfer Capacitance	C <sub>rss</sub>			66			
-		$V_{DS} = 20 \text{ V}$ . $V_{CS} = 10 \text{ V}$ . $I_{D} = 10 \text{ A}$		21.3	32	nC	
Total Gate Charge	Qg			9.8	15		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 20$ V, $V_{GS} = 4.5$ V, $I_{D} = 10$ A		3.2			
Gate-Drain Charge	Q <sub>gd</sub>			2.5			
Output Charge	Q <sub>oss</sub>	$V_{DS} = 20 V, V_{GS} = 0 V$		32	48		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.2	0.9	1.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			22	44		
Rise Time	t <sub>r</sub>	$V_{DD} = 20 V, R_1 = 2 \Omega$		65	120	1	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, \text{ R}_g = 1 \Omega$		24	45		
Fall Time	t <sub>f</sub>			9	18		
Turn-On Delay Time	t <sub>d(on)</sub>			11	22	- ns -	
Rise Time	t <sub>r</sub>	$V_{DD} = 20 \text{ V}, \text{ R}_{\text{I}} = 2 \Omega$		11	22		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	44		
Fall Time	t <sub>f</sub>			9	18		
Drain-Source Body Diode Characteristic						1	
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			40	Γ.	
Pulse Diode Forward Current (t = $100 \ \mu s$ )	I <sub>SM</sub>	-			100	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V		0.75	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			31	60	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			17	34	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$		13		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			18			

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

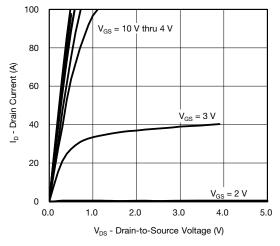
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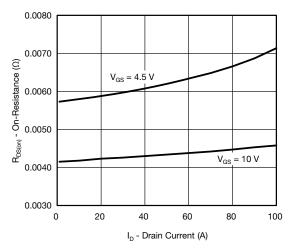
## FDMC8015L-VB



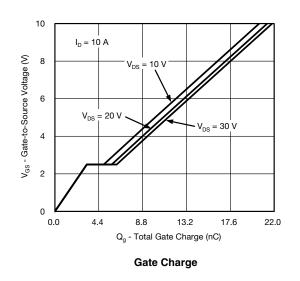
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

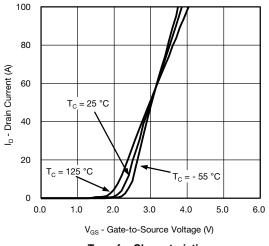




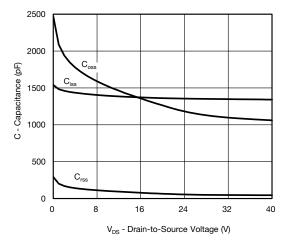


**On-Resistance vs. Drain Current and Gate Voltage** 

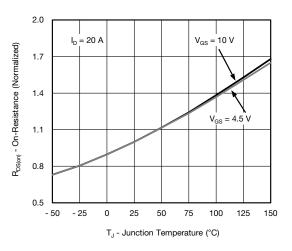




**Transfer Characteristics** 



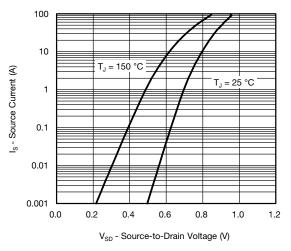
Capacitance

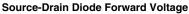


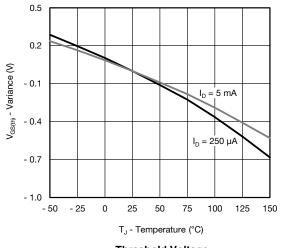
**On-Resistance vs. Junction Temperature** 



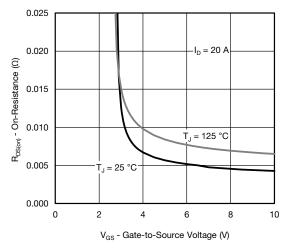
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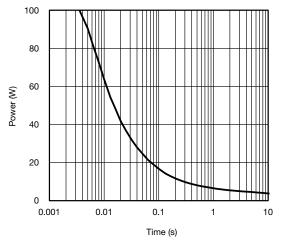




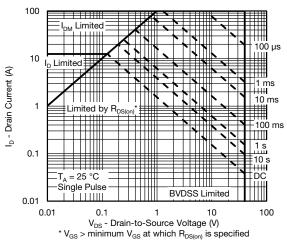
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage



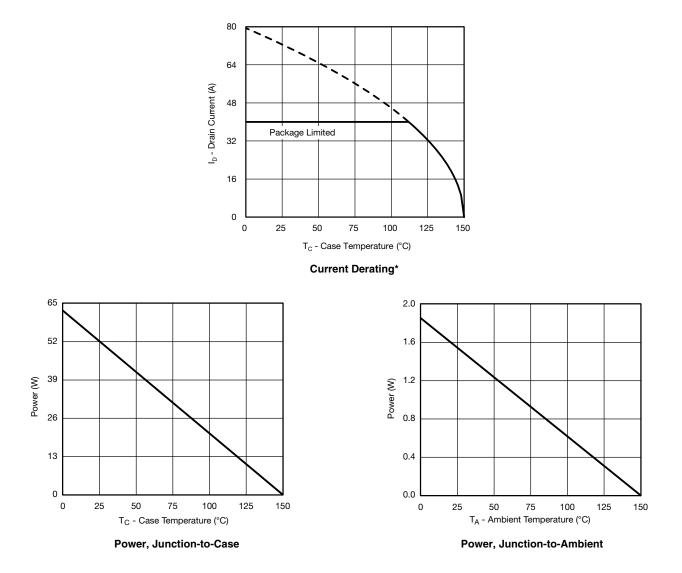
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient



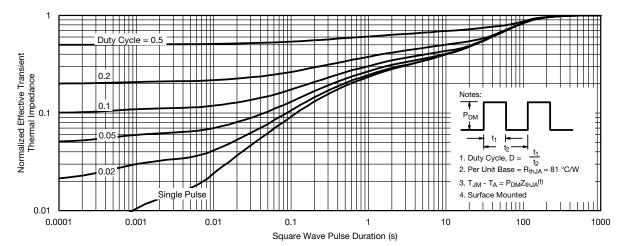
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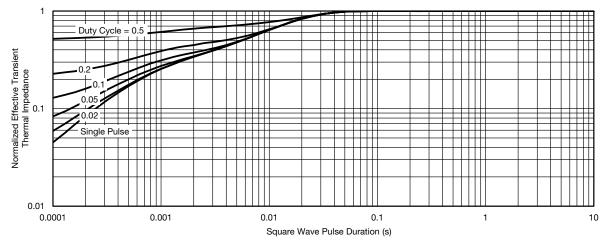
\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150 \text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

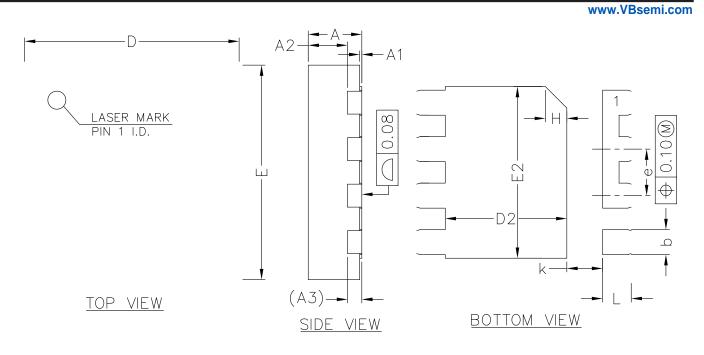


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

## FDMC8015L-VB





<u>SIDE VIEW</u>

SYMBOL	MIN	NOM	MAX		
А	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.50	0.55	0.60		
A3	0.20REF				
b	0.30	0.35	0.40		
D	2.90	3.00	3.10		
E	2.90	3.00	3.10		
D2	1.60	1.70	1.80		
E2	2.30	2.40	2.50		
е	0.55	0.65	0.75		
K	0.40	0.50	0.60		
L	0.35	0.40	0.45		

# COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)

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