

DMT3009LFVWQ-13-VB Datasheet

N-Channel 30-V (D-S) MOSFET

V_{DS}		30	V
$R_{DS(on),typ}$	$V_{GS}=10V$	13	$m\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	19	$m\Omega$
I_D		30	A

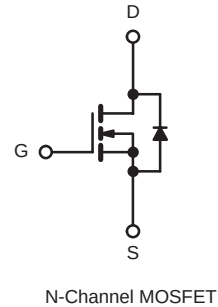
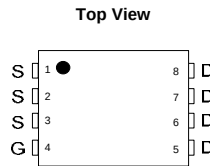
FEATURES

- Halogen-free
- Trench Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- DC/DC Conversion
- Low-Side Switch
- Notebook PC
- Gaming



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	30
		$T_C = 70^\circ\text{C}$	20
		$T_A = 25^\circ\text{C}$	21.5 ^{b, c}
		$T_A = 70^\circ\text{C}$	17.1 ^{b, c}
Pulsed Drain Current	I_{DM}	100	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	13
		$T_A = 25^\circ\text{C}$	3.1 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	10	A
Avalanche Energy	E_{AS}	5	mJ
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	60
		$T_C = 70^\circ\text{C}$	30
		$T_A = 25^\circ\text{C}$	3.7 ^{b, c}
		$T_A = 70^\circ\text{C}$	2.4 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	27	34	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	R_{thJF}	6	7.5	$^\circ\text{C/W}$

Notes:

- Based on $T_C = 25^\circ\text{C}$.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under Steady State conditions is 85°C/W .

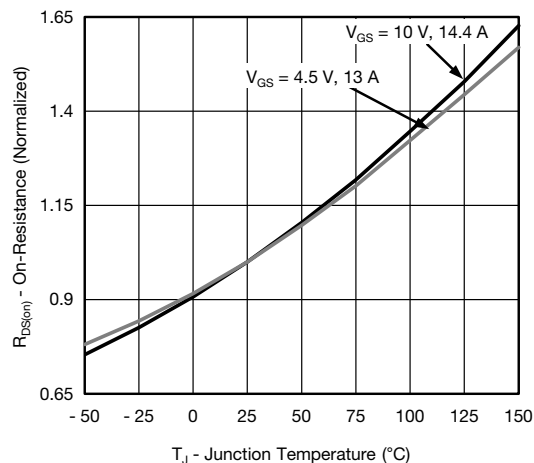
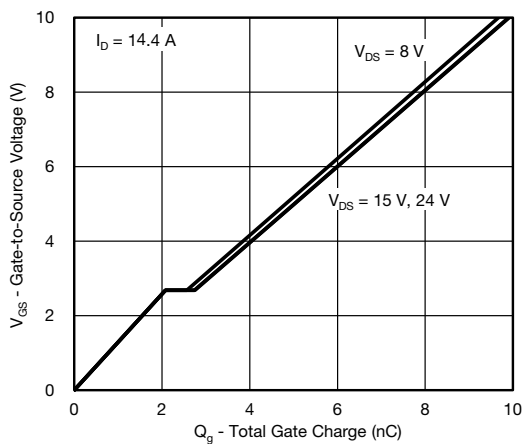
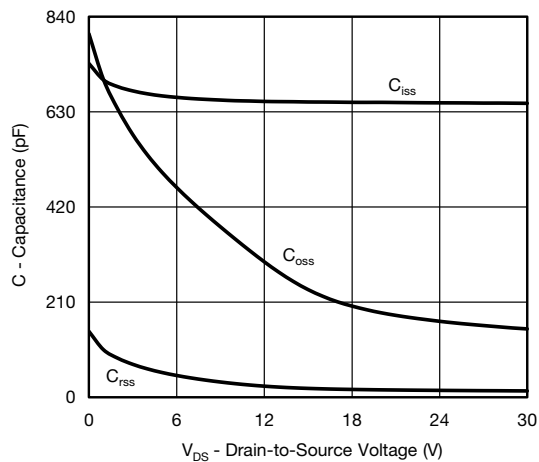
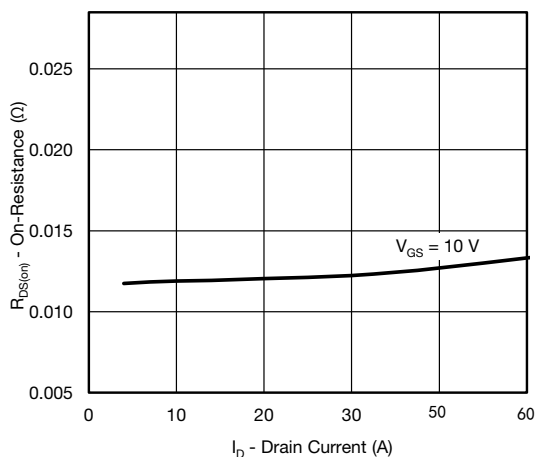
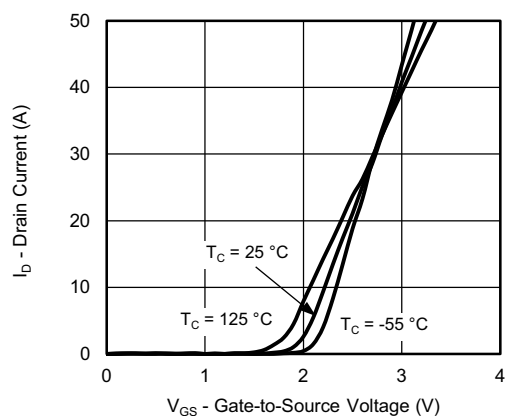
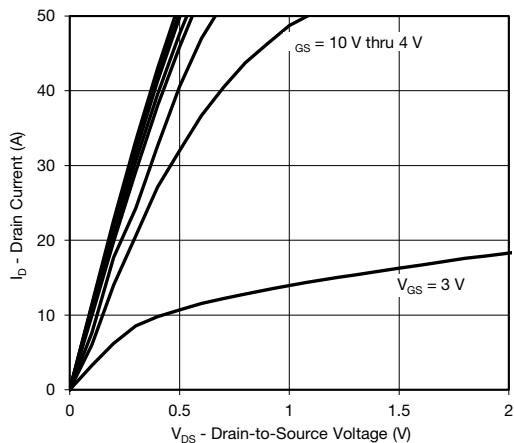
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		27		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		13		mΩ
		V _{GS} = 4.5 V, I _D = 10 A		19		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A		75		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz			900	pF
Output Capacitance	C _{oss}				236	
Reverse Transfer Capacitance	C _{rss}				20	
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A			20	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A			9	
Gate-Source Charge	Q _{gs}				2.1	
Gate-Drain Charge	Q _{gd}				0.7	
Gate Resistance	R _g	f = 1 MHz	0.2	1.1	2.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		8	16	ns
Rise Time	t _r			16	30	
Turn-Off Delay Time	t _{d(off)}			17	35	
Fall Time	t _f			7	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		14	30	
Rise Time	t _r			50	100	
Turn-Off Delay Time	t _{d(off)}			16	30	
Fall Time	t _f			8	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			13	A
Pulse Diode Forward Current ^a	I _{SM}				100	
Body Diode Voltage	V _{SD}	I _S = 3 A			1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C			40	ns
Body Diode Reverse Recovery Charge	Q _{rr}				20	nC
Reverse Recovery Fall Time	t _a			12.5		ns
Reverse Recovery Rise Time	t _b			7.5		

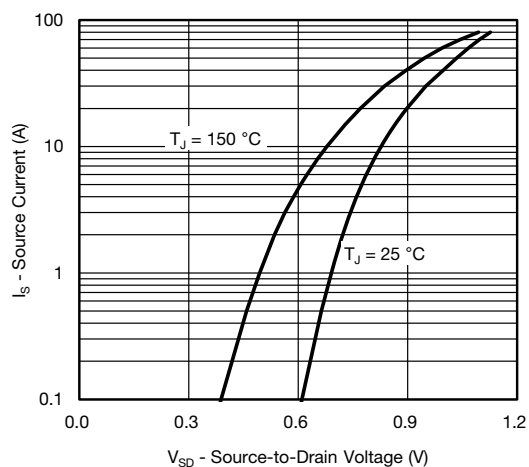
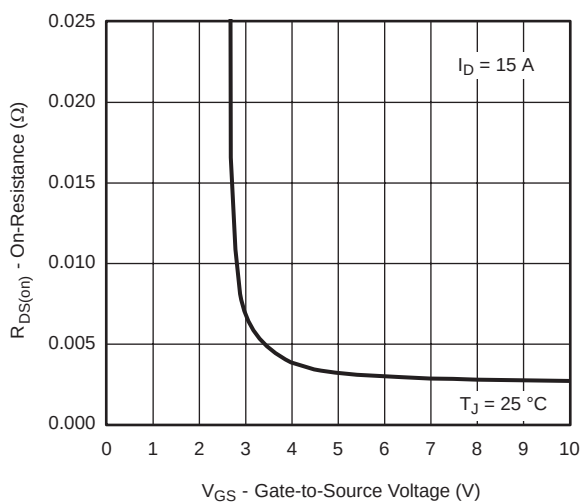
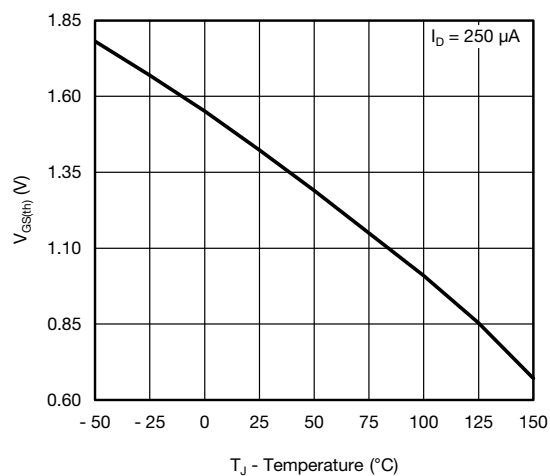
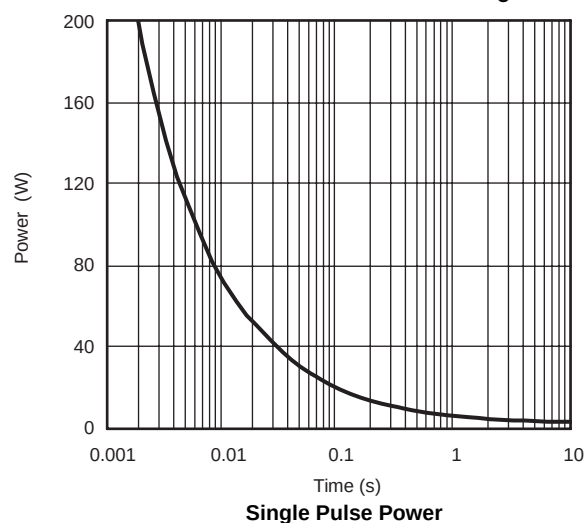
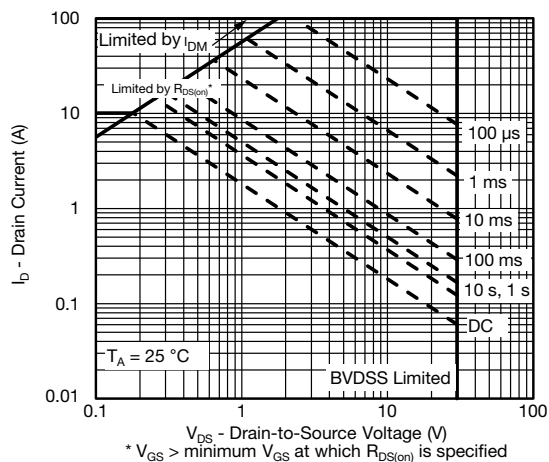
Notes:

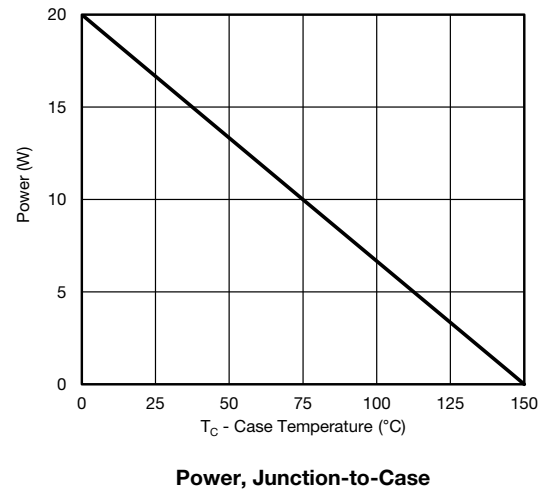
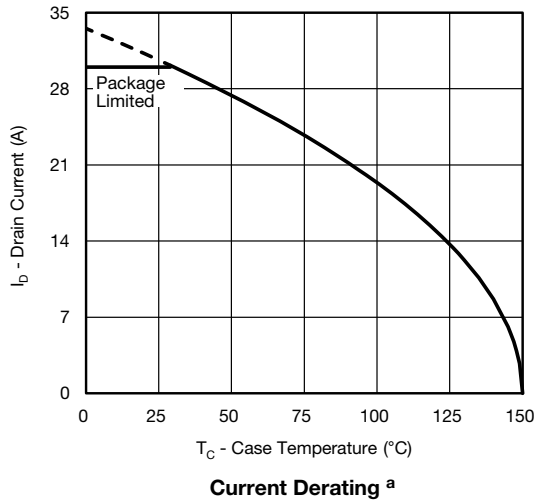
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

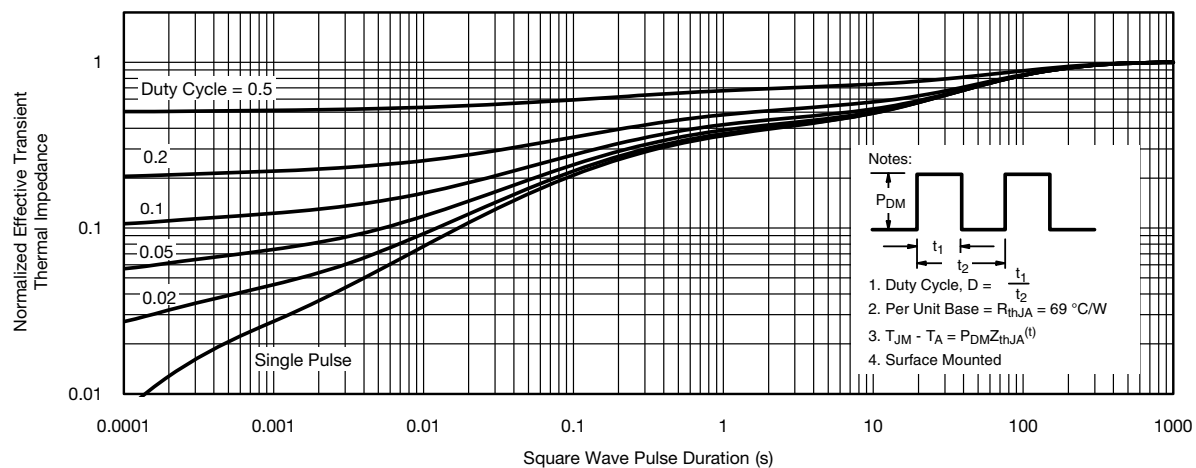
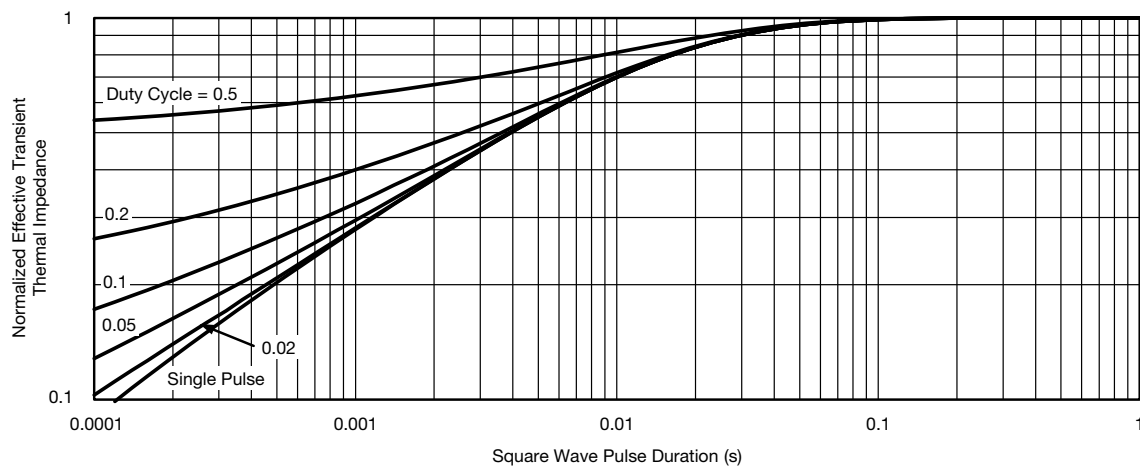
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


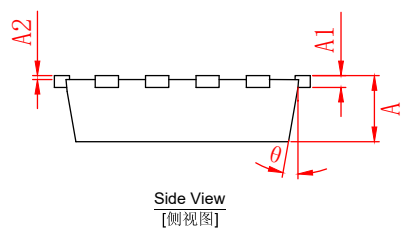
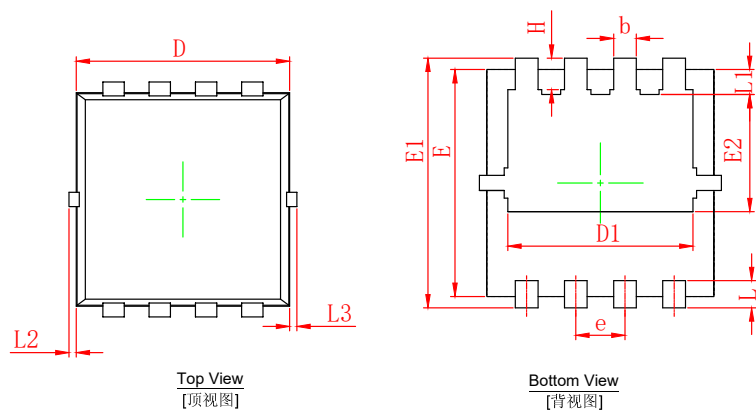
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Note**

- a. The power dissipation P_D is based on $T_J \text{ max.} = 25^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

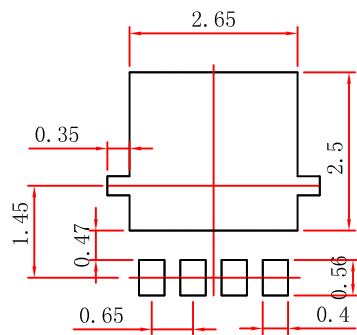
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

PDFNWB3×3-8L Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



- Note:
- 1.Controlling dimension:in millimeters.
 - 2.General tolerance:±0.05mm.
 - 3.The pad layout is for reference purposes only.

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