

CSD25404Q3T-VB Datasheet

P-Channel 20V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.004 at $V_{GS} = -4.5$ V	- 52 ^a	58 nC
	0.005 at $V_{GS} = -2.5$ V	- 42 ^a	

FEATURES

- Trench Power MOSFET
- Thermally Enhanced DFN3X3 Package
- Low On-Resistance for Low Voltage Drop

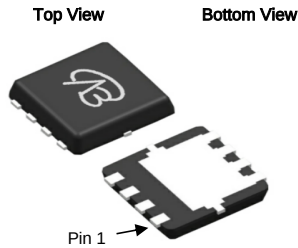


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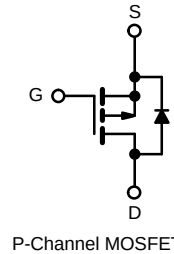
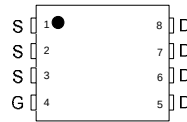
APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Devices

DFN 3x3



Top View



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current ($t = 300 \mu\text{s}$)	I_{DM}	- 208	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	- 29 ^{b, c}
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	18	26	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	1.3	1.5	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- See solder profile The DFN3X3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80°C/W .

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 11		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.8		- 2	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 12 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 12 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 5.3 A		0.004		Ω
		V _{GS} = - 4.5 V, I _D = - 8.1 A		0.0045		
		V _{GS} = - 2.5 V, I _D = - 5.3 A		0.005		
		V _{GS} = - 2.5 V, I _D = - 6 A		0.0054		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 18.5 A		94		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		4600		pF
Output Capacitance	C _{oss}			830		
Reverse Transfer Capacitance	C _{rss}			570		
Total Gate Charge	Q _g	V _{DS} = - 6 V, V _{GS} = - 8 V, I _D = - 10 A		58	97	nC
Gate-Source Charge	Q _{gs}	V _{DS} = - 6 V, V _{GS} = - 4.5 V, I _D = - 10 A		33	65	
Gate-Drain Charge	Q _{gd}			7		
				15.5		
Gate Resistance	R _g	f = 1 MHz		5		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 6 V, R _L = 0.75 Ω I _D ≅ - 8 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			40	60	
Turn-Off Delay Time	t _{d(off)}			65	100	
Fall Time	t _f			40	60	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 6 V, R _L = 0.75 Ω I _D ≅ - 8 A, V _{GEN} = - 8 V, R _g = 1 Ω		10	15	
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			70	105	
Fall Time	t _f			40	60	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 52	A
Pulse Diode Forward Current	I _{SM}				200	
Body Diode Voltage	V _{SD}	I _S = - 8 A, V _{GS} = 0 V		- 0.57	- 1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 8 A, di/dt = 100 A/μs, T _J = 25 °C		40	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			20	30	nC
Reverse Recovery Fall Time	t _a			14		ns
Reverse Recovery Rise Time	t _b			26		

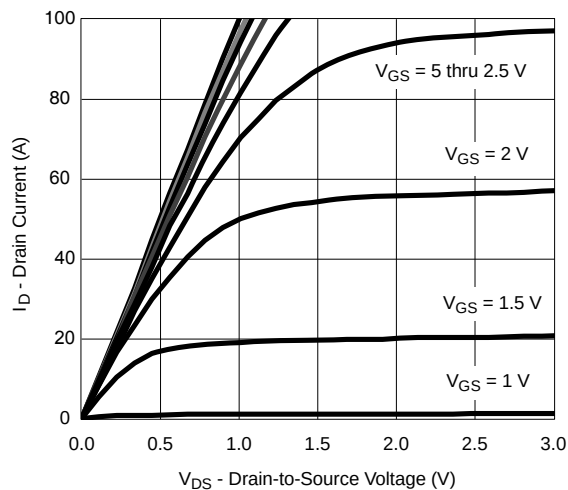
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

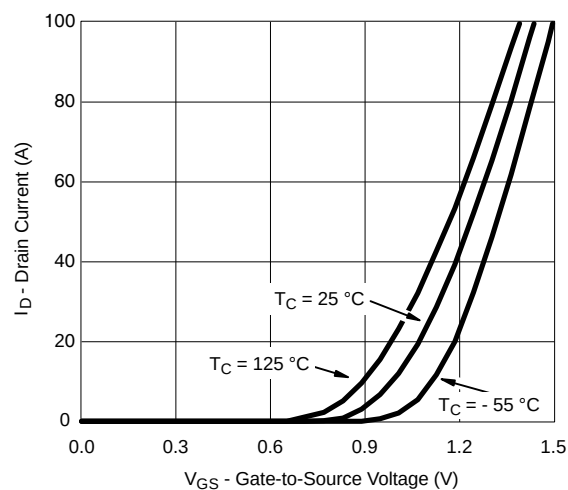
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

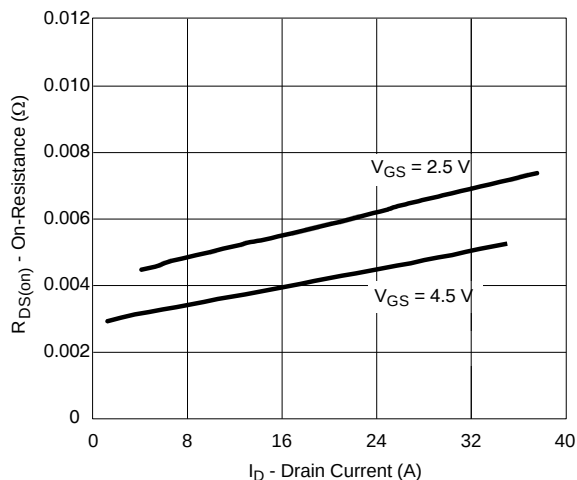
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



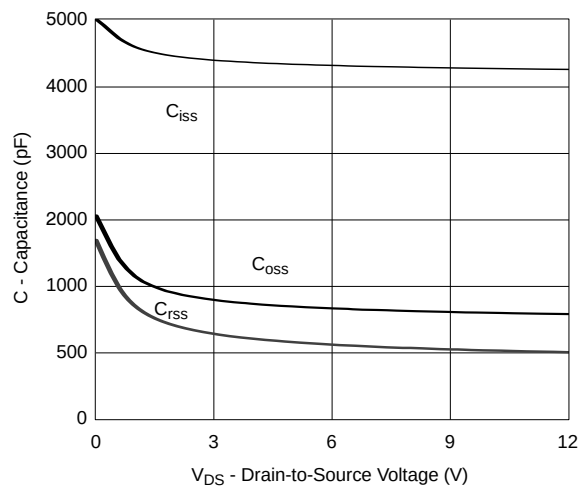
Output Characteristics



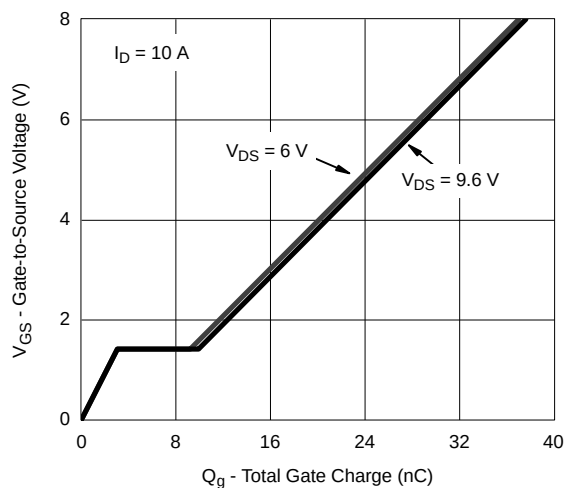
Transfer Characteristics



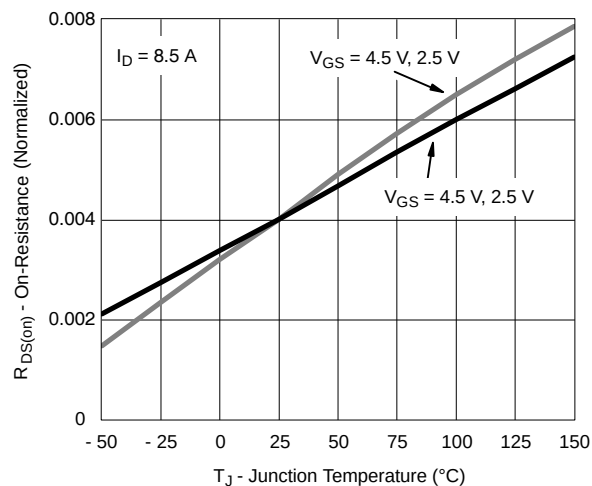
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

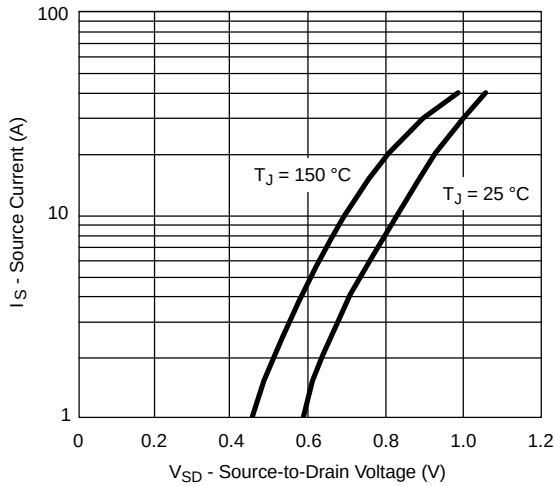


Gate Charge

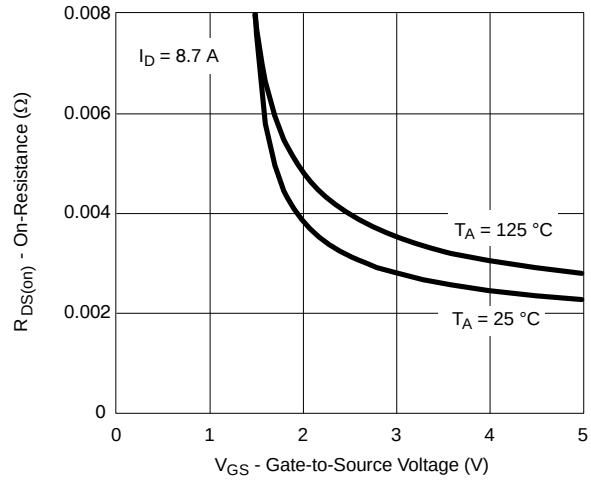


On-Resistance vs. Junction Temperature

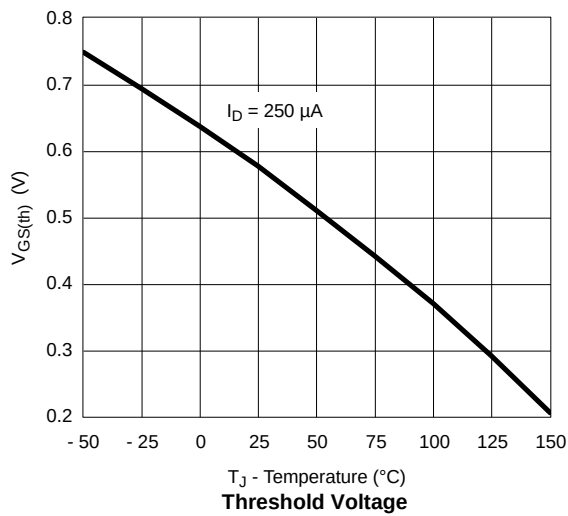
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



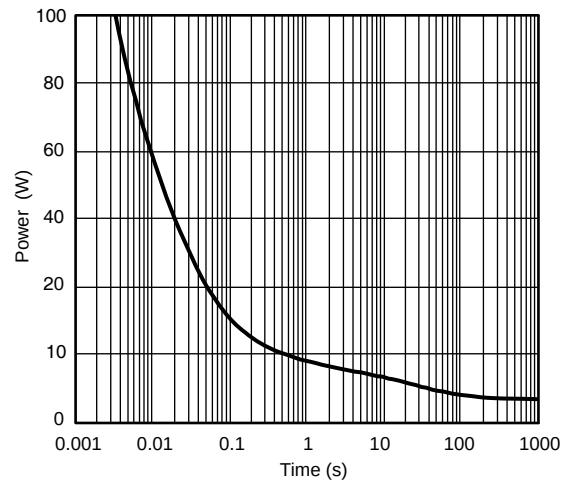
Source-Drain Diode Forward Voltage



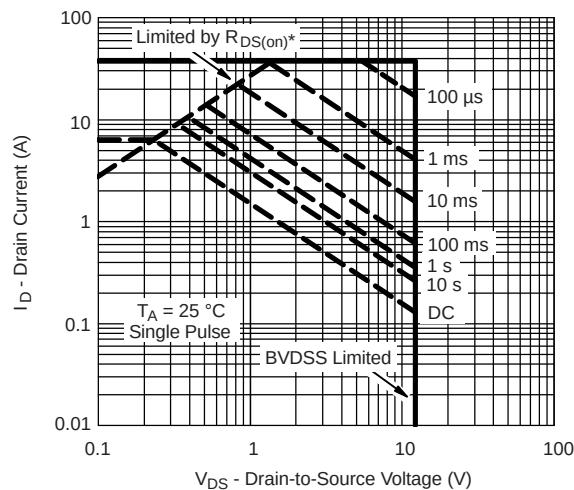
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

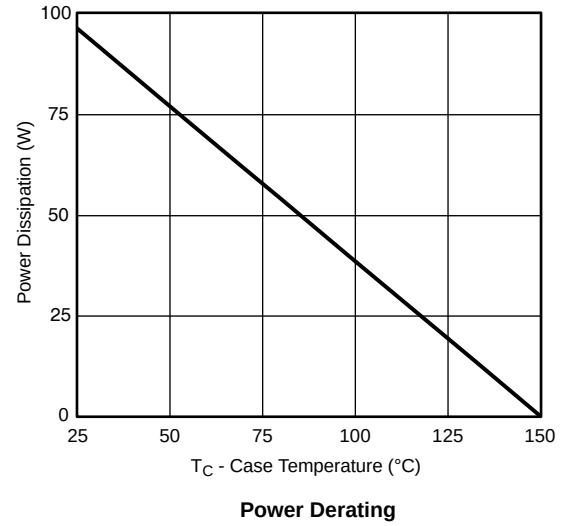
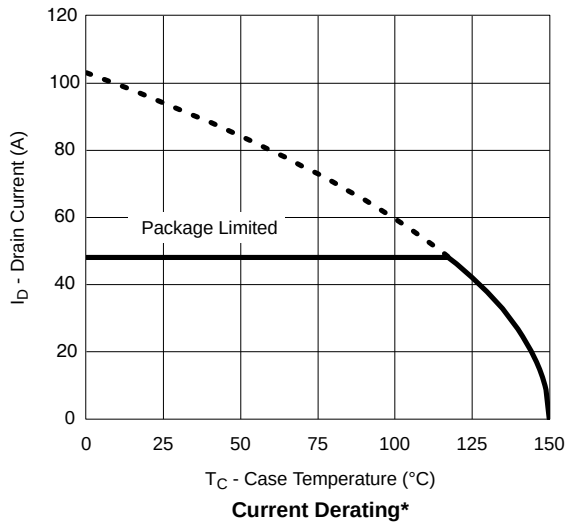


Single Pulse Power, Junction-to-Ambient



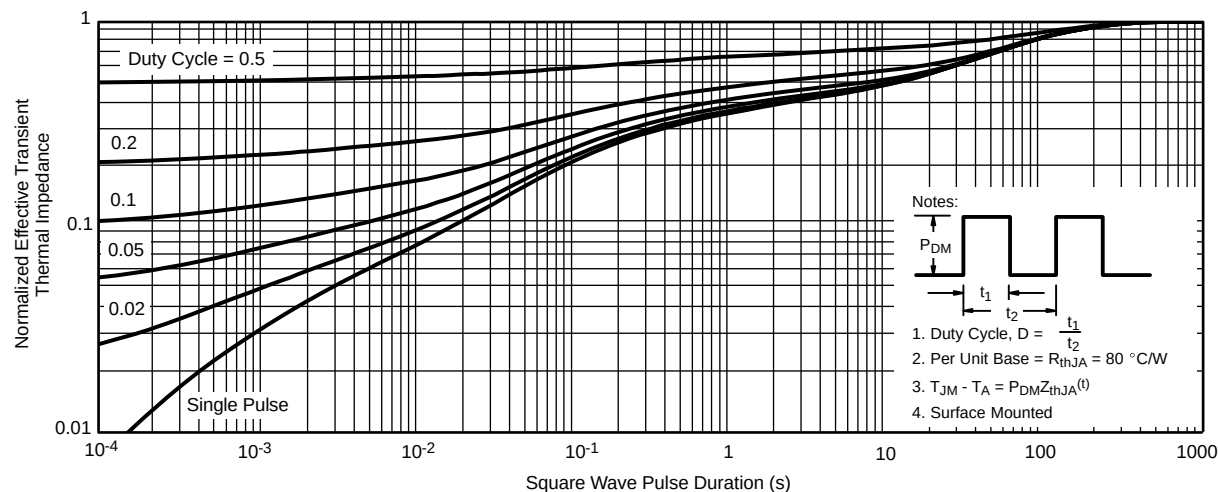
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

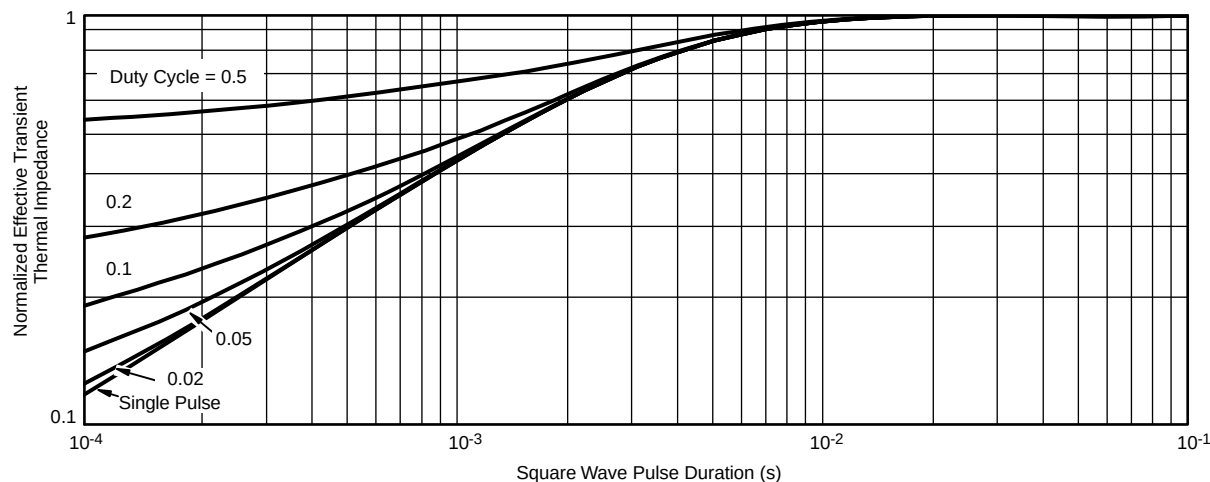


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

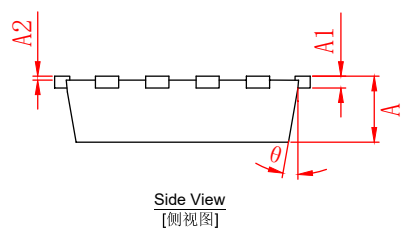
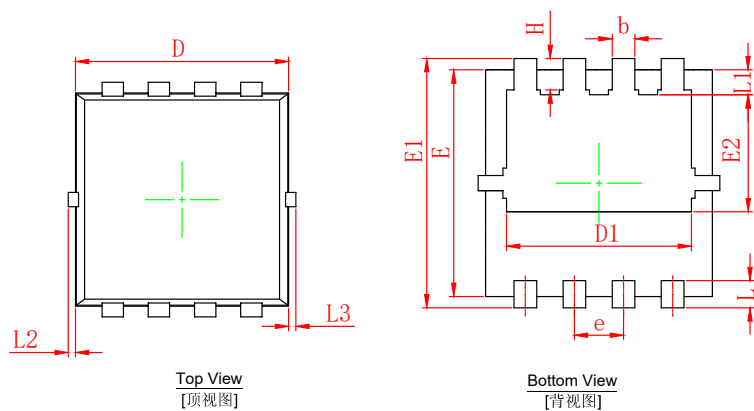


Normalized Thermal Transient Impedance, Junction-to-Ambient



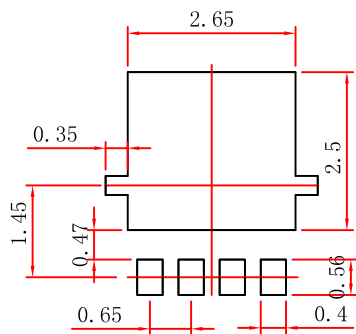
Normalized Thermal Transient Impedance, Junction-to-Case

PDFNWB3×3-8L Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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