

## AON7409-VB Datasheet P-Channel 30 V (D-S) MOSFET

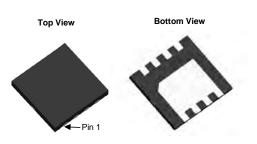
V <sub>DS</sub>		-30	V
R <sub>DS(on),typ</sub>	V <sub>GS</sub> =10V	11	mΩ
R <sub>DS(on),typ</sub>	V <sub>GS</sub> =4.5V	18	mΩ
ID	-45	А	

#### FEATURES

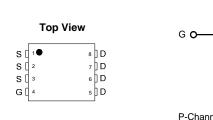
- Halogen-free According to IEC 61249-2-21
  Definition
- Trench Power MOSFET
- Low Thermal Resistance Power
  Package with Small Size and Low 1.07 mm
  Profile
- 100  $\%~\text{R}_{g}$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

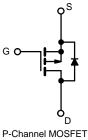
#### **APPLICATIONS**

- · Load Switch
- Adaptor Switch
- Notebook PC



DFN 3x3 EP





Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	- 30	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
	T <sub>C</sub> = 25 °C		- 45		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C		- 30		
Continuous Drain Current $(1) = 150^{\circ}$ C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 14.4 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		- 11.5 <sup>a, b</sup>	•	
Pulsed Drain Current	I <sub>DM</sub>	- 60	— A		
Continuous Source Drain Diado Current	T <sub>C</sub> = 25 °C	1.	- 35 <sup>e</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	- 3.2 <sup>a, b</sup>		
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	- 25		
Single-Pulse Avalanche Energy	L = 0.1 MH	E <sub>AS</sub>	31.25	mJ	
	T <sub>C</sub> = 25 °C		52		
Maximum Bower Dissinction	T <sub>C</sub> = 70 °C	P <sub>D</sub>	43	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	'D	3.8 <sup>a, b</sup>	vv	
	T <sub>A</sub> = 70 °C		2.4 <sup>a, b</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>c, d</sup>			260		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c.Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

d.Package limited.

e.Based on T  $_{\rm C}$  = 25 °C



COMPLIANT

HALOGEN

FREE



THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, b</sup>	t ≤ 10 s	R <sub>thJA</sub>	26	33	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.9	2.4	0/10	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 81 °C/W.

<b>SPECIFICATIONS</b> ( $T_J = 25 \degree C$				_			
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				-	1		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = -250 \mu A$	- 30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 20		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	5 .		5			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$	- 1.5		- 2.8	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	laaa	$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$			- 10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 V$ , $V_{GS} = -10 V$	- 20			Α	
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 14.4 A		11		mΩ	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 11.5 A		18			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 14.4 A		37		S	
Dynamic <sup>b</sup>		· · · · · · · · · · · · · · · · · · ·					
Input Capacitance	C <sub>iss</sub>			2000		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		385			
Reverse Transfer Capacitance	C <sub>rss</sub>			322			
	tal Gate Charge $Q_g = \frac{V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, V_{SS} = -10 \text{ V}, $	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -14.4 \text{ A}$			15		
Total Gate Charge					14	- nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -14.4 \text{ A}$			7		
Gate-Drain Charge	Q <sub>gd</sub>				9		
Gate Resistance	R <sub>q</sub>	f = 1 MHz	0.4	1.8	3.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			50	75		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_{L}$ = 1.5 $\Omega$		43	65	-	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong$ - 10 A, $V_{GEN}$ = - 4.5 V, $R_q$ = 1 $\Omega$		30	45		
Fall Time	t <sub>f</sub>			14	21		
Turn-On Delay Time	t <sub>d(on)</sub>			14	21	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_{L}$ = 1.5 $\Omega$		9	18	-	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong$ - 10 A, $V_{GEN}$ = - 10 V, $R_q$ = 1 $\Omega$		36	54		
Fall Time	t <sub>f</sub>			10	20	1	
Drain-Source Body Diode Characterist	ics	1				1	
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			- 35 <sup>e</sup>		
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	-			- 60	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>F</sub> = - 10 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	· · · · · · · · · · · · · · · · · · ·		31	47	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1		30	45	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	I <sub>F</sub> = - 10 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		15			
	t <sub>b</sub>			.0		ns	

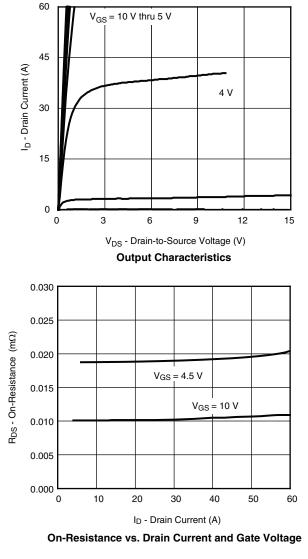
Notes:

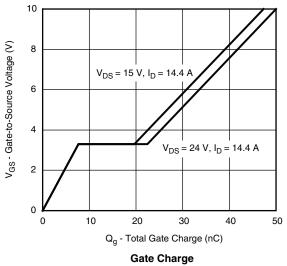
a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

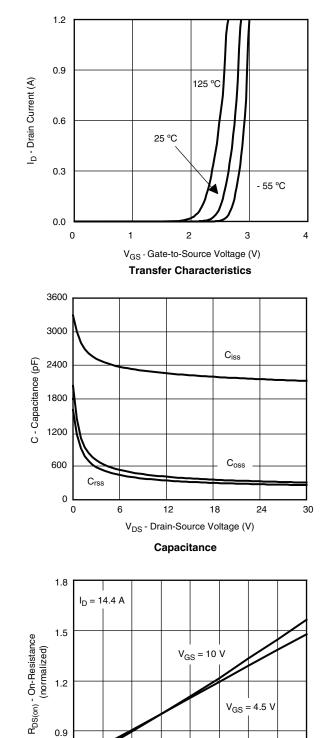
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.









0.6 **–** - 50

- 25

25

0

50

T<sub>J</sub> - Junction Temperature (°C) On-Resistance vs. Junction Temperature

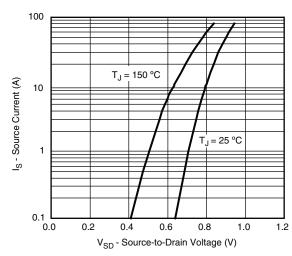
100

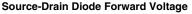
75

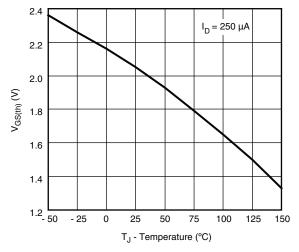
125

150

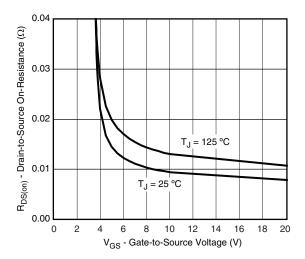




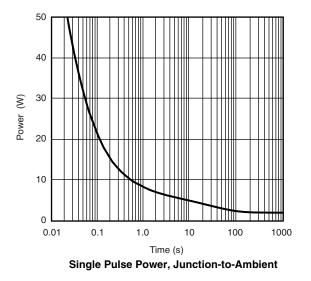


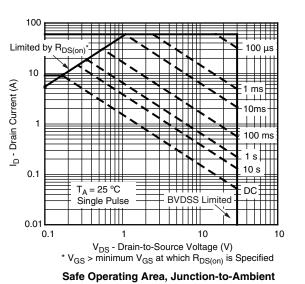


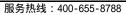
**Threshold Voltage** 



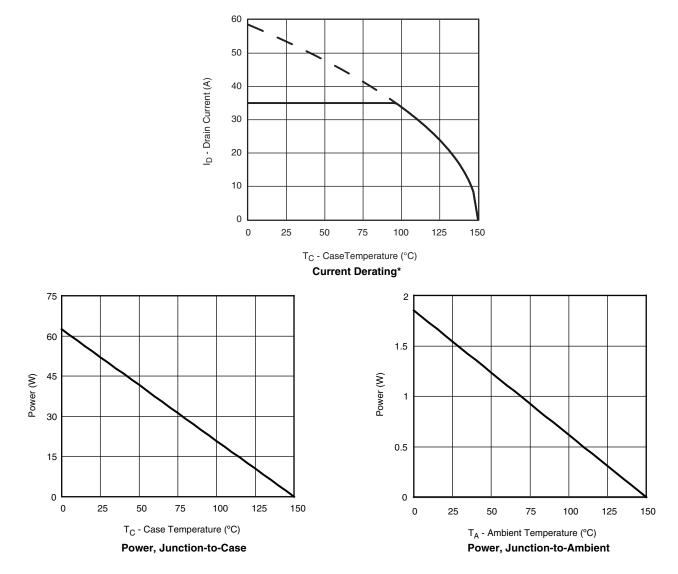
On-Resistance vs. Gate-to-Source Voltage





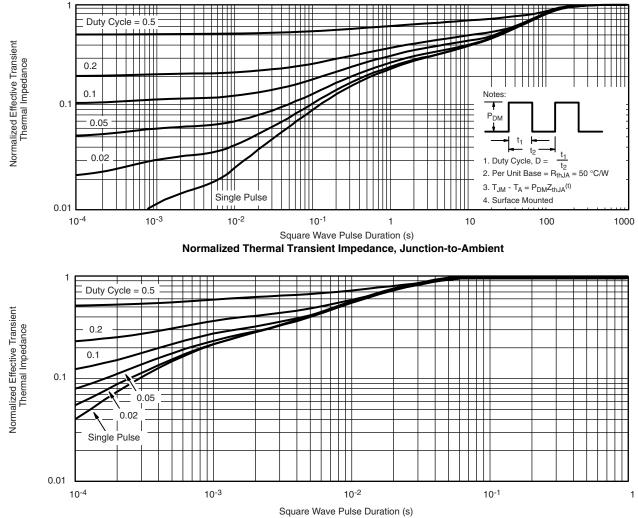






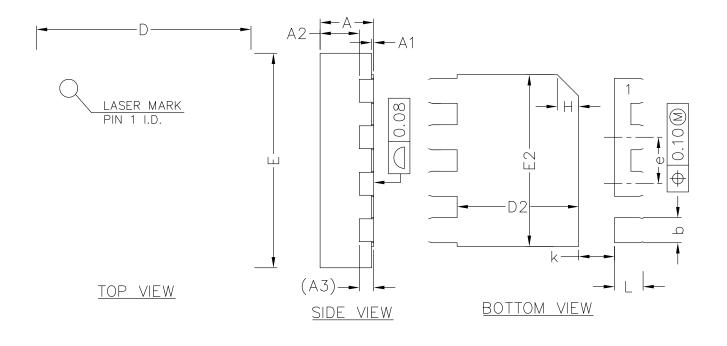
\* The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Case

WBsemi www.VBsemi.com





<u>SIDE VIEW</u>

× ·					
SYMBOL	MIN	NOM	MAX		
А	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.50	0.55	0.60		
A3	0.20REF				
b	0.30	0.35	0.40		
D	2.90	3.00	3.10		
E	2.90	3.00	3.10		
D2	1.60	1.70	1.80		
E2	2.30	2.40	2.50		
е	0.55	0.65	0.75		
К	0.40	0.50	0.60		
L	0.35	0.40	0.45		

### COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)



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