

HT8KE5TB1-VB Datasheet

DualN-Channel 100V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^f	Q_g (Typ.)
100	0.071 at $V_{GS} = 10$ V	12.1	3.3 nC
	0.076 at $V_{GS} = 7.5$ V	11.8	
	0.086 at $V_{GS} = 6$ V	10.9	

FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- DC/DC Conversion
- Primary side switch
- Synchronous Rectification
- Industrial
- 48 V Battery Monitoring
- LED Driver

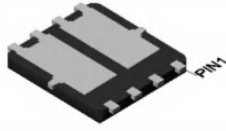


RoHS
COMPLIANT
HALOGEN
FREE

DFN8(3x3)-B

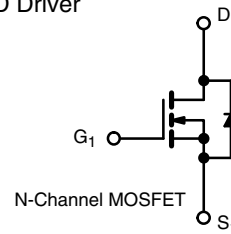


Top View

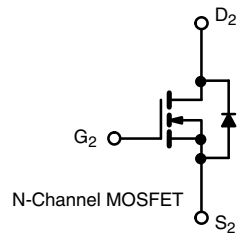


Bottom View

Top View



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	12.1
		$T_C = 70^\circ\text{C}$	9.7
		$T_A = 25^\circ\text{C}$	4.1 ^{a, b}
		$T_A = 70^\circ\text{C}$	3.2 ^{a, b}
Pulsed Drain Current ($t = 300 \mu\text{s}$)	I_{DM}	20	
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	20
		$T_A = 25^\circ\text{C}$	2.3 ^{a, b}
Single Pulse Avalanche Current	I_{AS}	7	
Single Pulse Avalanche Energy	E_{AS}	2.5	mJ
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	25
		$T_C = 70^\circ\text{C}$	16
		$T_A = 25^\circ\text{C}$	2.8 ^{a, b}
		$T_A = 70^\circ\text{C}$	1.8 ^{a, b}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, e}	R_{thJA}	35	44	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	4	5	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. $t = 10$ s.

c. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Maximum under steady state conditions is 94°C/W .

f. Based on $T_C = 25^\circ\text{C}$.

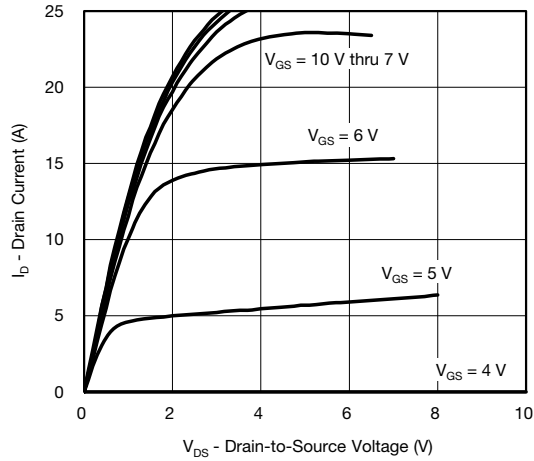
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		61		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6.2		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	8			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 8 A		0.071		Ω
		V _{GS} = 7.5 V, I _D = 6 A		0.076		
		V _{GS} = 6 V, I _D = 4 A		0.086		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 8 A		11		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		250		pF
Output Capacitance	C _{oss}			73		
Reverse Transfer Capacitance	C _{rss}			7		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A		5.2	8	nC
		V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 10 A		4	6	
		V _{DS} = 50 V, V _{GS} = 6 V, I _D = 10 A		3.3	5	
Gate-Source Charge	Q _{gs}			1.4		
Gate-Drain Charge	Q _{gd}			1.5		
Output Charge	Q _{oss}	V _{DS} = 50 V, V _{GS} = 0 V		7	11	
Gate Resistance	R _g	f = 1 MHz	1	3.1	5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω		8	16	ns
Rise Time	t _r			8	16	
Turn-Off Delay Time	t _{d(off)}			8	16	
Fall Time	t _f			6	12	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		7	14	
Rise Time	t _r			7	14	
Turn-Off Delay Time	t _{d(off)}			8	16	
Fall Time	t _f			5	10	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			20	A
Pulse Diode Forward Current	I _{SM}				20	
Body Diode Voltage	V _{SD}	I _S = 4 A, V _{GS} = 0 V		0.87	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			27	54	nC
Reverse Recovery Fall Time	t _a			16		ns
Reverse Recovery Rise Time	t _b			14		

Notes:

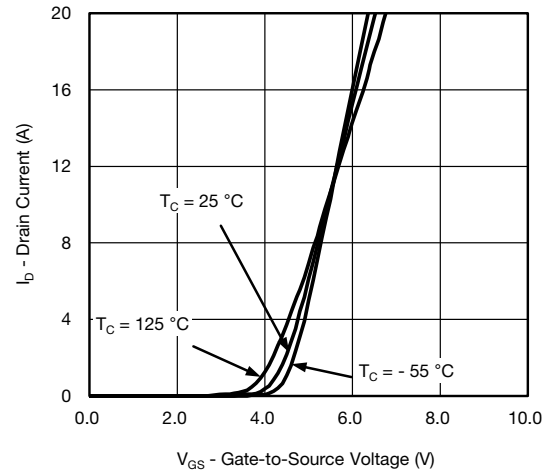
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

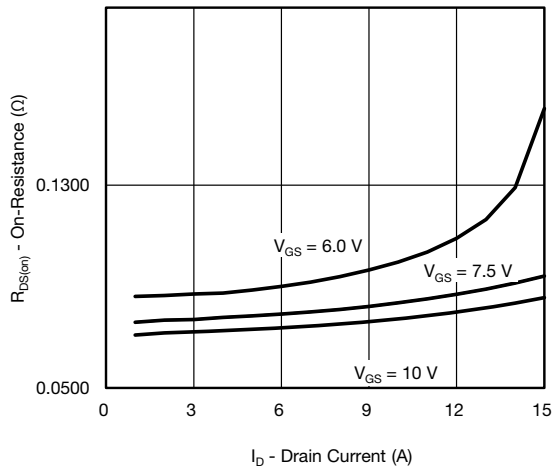
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



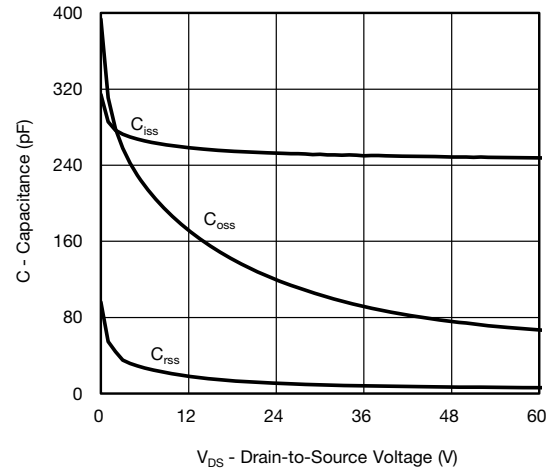
Output Characteristics



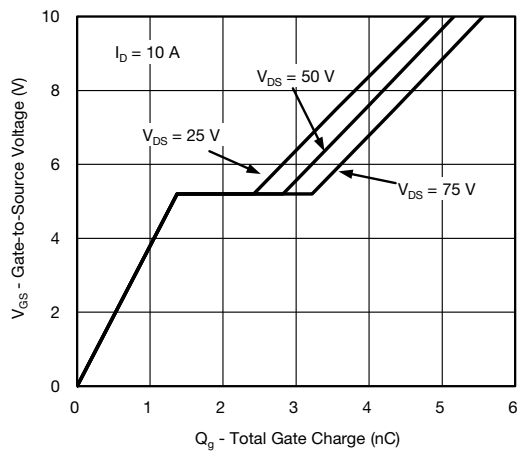
Transfer Characteristics



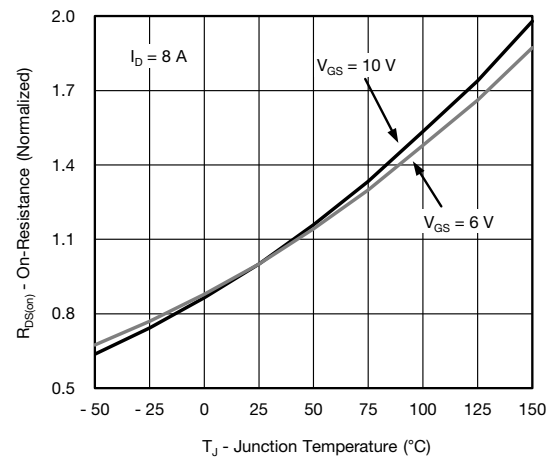
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

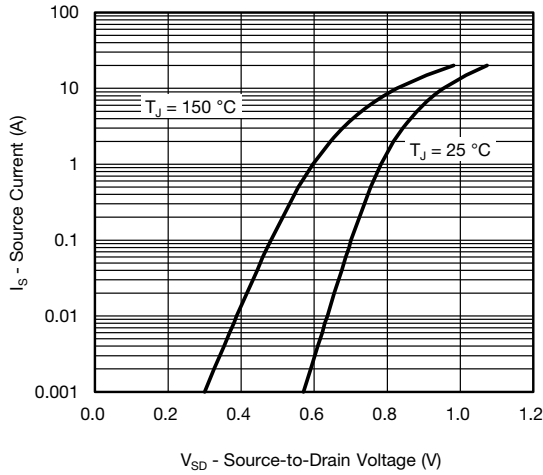


Gate Charge

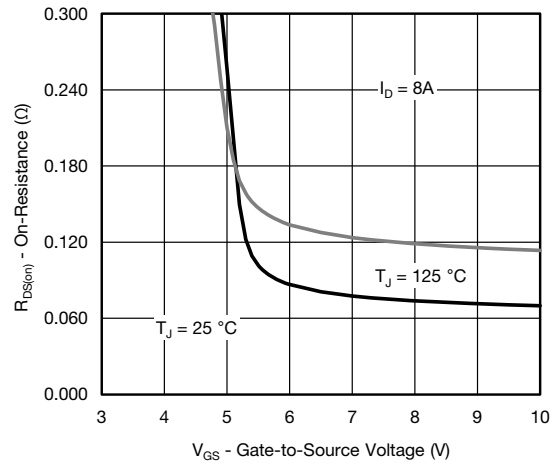


On-Resistance vs. Junction Temperature

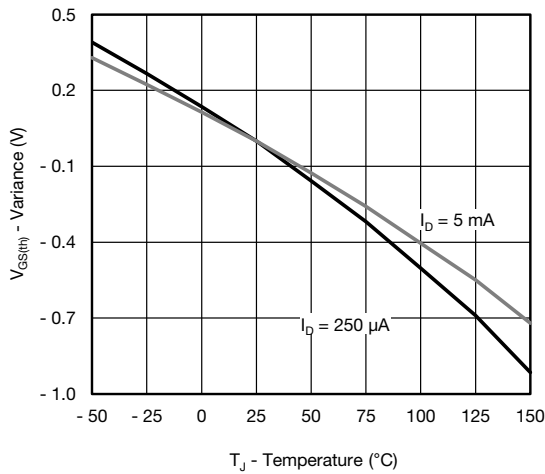
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



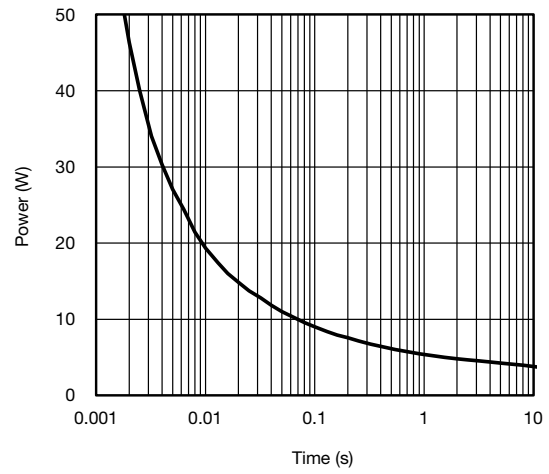
Source-Drain Diode Forward Voltage



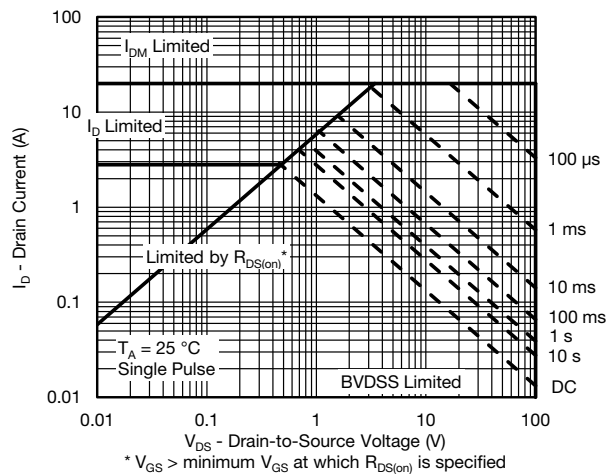
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

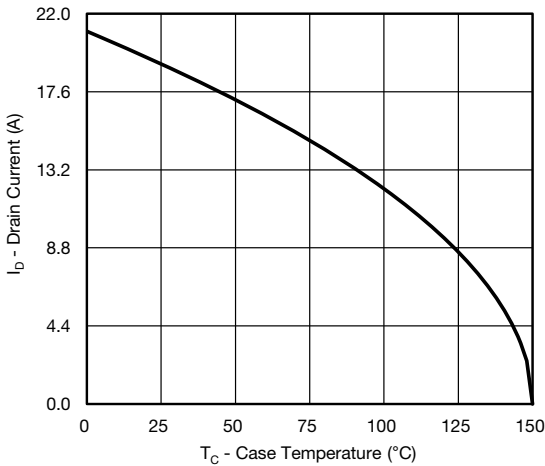


Single Pulse Power, Junction-to-Ambient

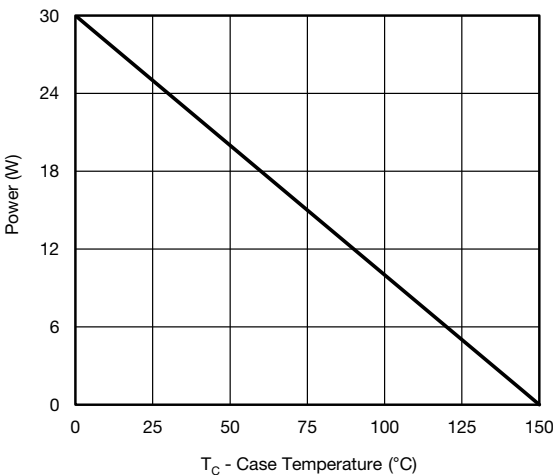


Safe Operating Area, Junction-to-Ambient

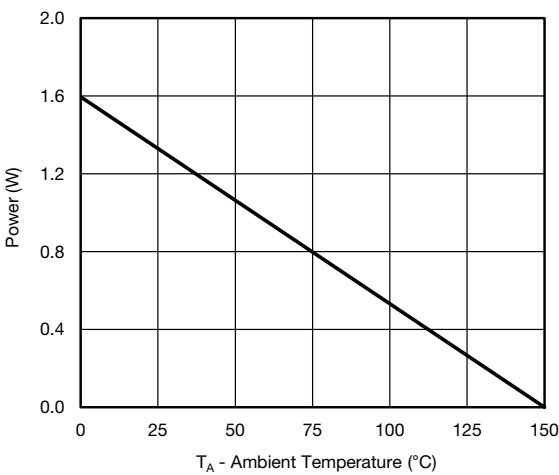
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



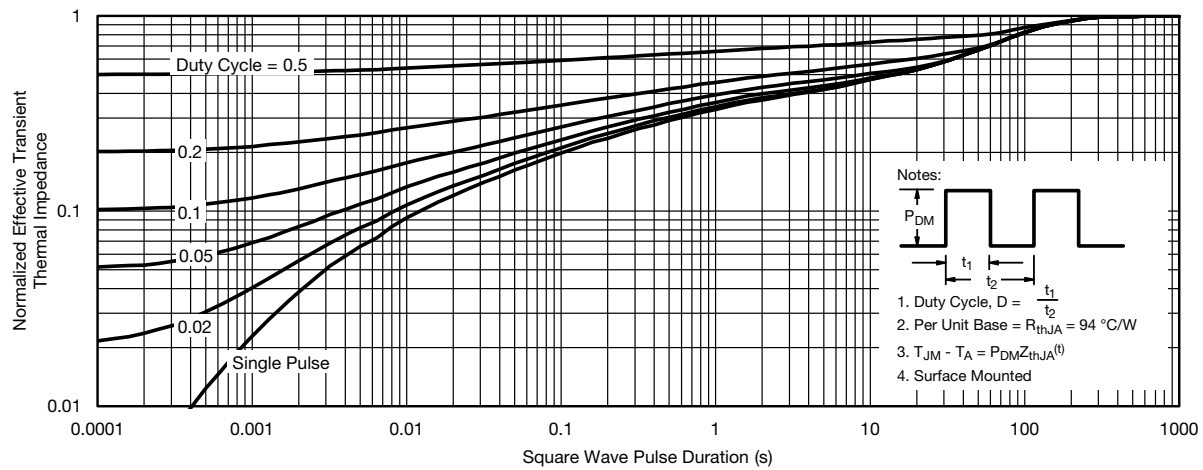
Power, Junction-to-Case



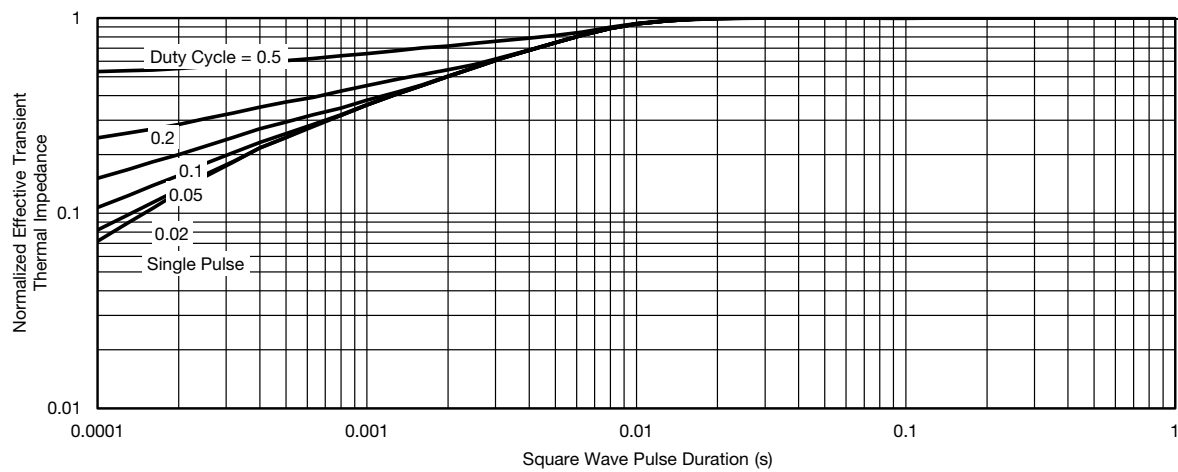
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

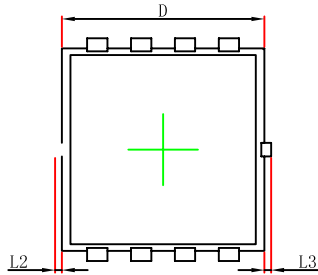


Normalized Thermal Transient Impedance, Junction-to-Ambient

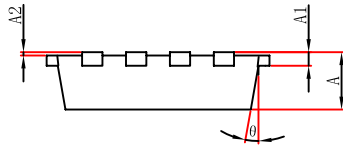
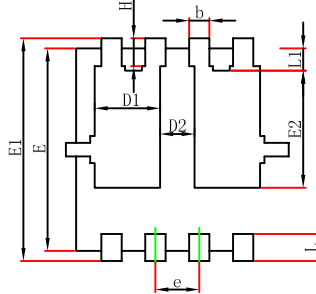


Normalized Thermal Transient Impedance, Junction-to-Case

PDFNWB3×3-8L-B Package Outline Dimensions



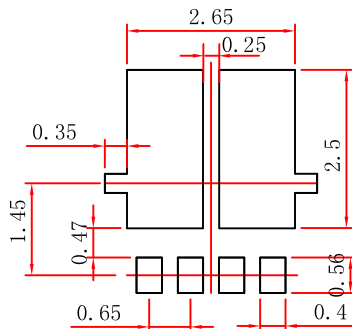
Top View
[顶视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	0.935	1.135	0.037	0.045
D2	0.280	0.480	0.011	0.019
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3×3-8L-B Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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