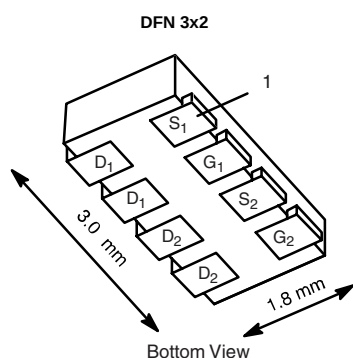


TPCF8402-VB Datasheet

Complementary 20 V (D-S) MOSFET

PRODUCT SUMMARY

	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.032 at $V_{GS} = 4.5$ V	5.9
		0.036 at $V_{GS} = 2.5$ V	5.6
		0.042 at $V_{GS} = 1.8$ V	5.2
P-Channel	- 20	0.069 at $V_{GS} = - 4.5$ V	- 4.1
		0.097 at $V_{GS} = - 2.5$ V	- 3.4
		0.137 at $V_{GS} = - 1.8$ V	- 2.9



FEATURES

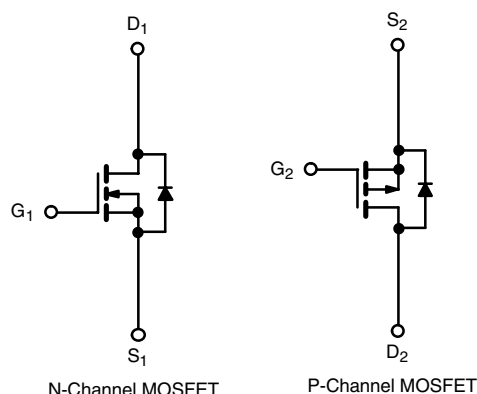
- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFETs
- Ultra Low $R_{DS(on)}$ and Excellent Power Handling In Compact Footprint
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switching for Portable Devices



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter		Symbol	N-Channel		P-Channel		Unit
			5 s	Steady State	5 s	Steady State	
Drain-Source Voltage		V _{DS}	20		- 20		V
Gate-Source Voltage		V _{GS}	± 8				
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	5.9	4.4	- 4.1	- 3	A
	T _A = 85 °C		4.2	3.1	- 2.9	- 2.2	
Pulsed Drain Current		I _{DM}	20		- 15		
Continuous Source Current (Diode Conduction) ^a		I _S	1.8	0.9	- 1.8	- 0.9	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.1	1.1	2.1	1.1	W
	T _A = 85 °C		1.1	0.6	1.1	0.6	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260				

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	60	$^\circ\text{C/W}$
		90	110	
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See Reliability Manual for profile. The DFN3x2 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Static								
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.4		1.0	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.4		-1.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	N-Ch P-Ch			± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^{\circ}\text{C}$	N-Ch			5		
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^{\circ}\text{C}$	P-Ch			-5		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	20			A	
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-15				
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 4.4\text{ A}$	N-Ch		0.032		Ω	
		$V_{GS} = -4.5\text{ V}, I_D = -3\text{ A}$	P-Ch		0.069			
		$V_{GS} = 2.5\text{ V}, I_D = 4.1\text{ A}$	N-Ch		0.036			
		$V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$	P-Ch		0.097			
		$V_{GS} = 1.8\text{ V}, I_D = 1.9\text{ A}$	N-Ch		0.042			
		$V_{GS} = -1.8\text{ V}, I_D = -0.6\text{ A}$	P-Ch		0.137			
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 4.4\text{ A}$	N-Ch		22		S	
		$V_{DS} = -10\text{ V}, I_D = -3\text{ A}$	P-Ch		8			
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.9\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V	
		$I_S = -0.9\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2		
Dynamic ^b								
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.4\text{ A}$	N-Ch		5	7.5	nC	
Gate-Source Charge	Q_{gs}		P-Ch		5.5	8.5		
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3\text{ A}$	N-Ch		0.85			
			P-Ch		0.91			
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 6\text{ }\Omega$	N-Ch		20	30	ns	
Rise Time	t_r		P-Ch		18	30		
			N-Ch		36	55		
Turn-Off Delay Time	$t_{d(off)}$		P-Ch		32	50		
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$	N-Ch		30	45		
			P-Ch		42	65		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 0.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$	N-Ch		12	20		
		$I_F = -0.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$	P-Ch		26	40		
					45	90		
					30	60		

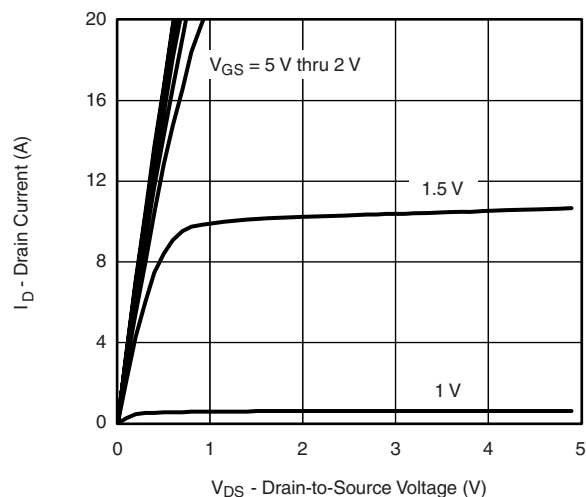
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

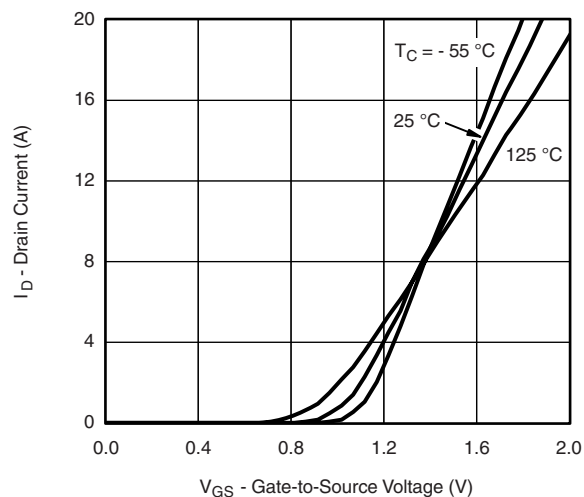
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

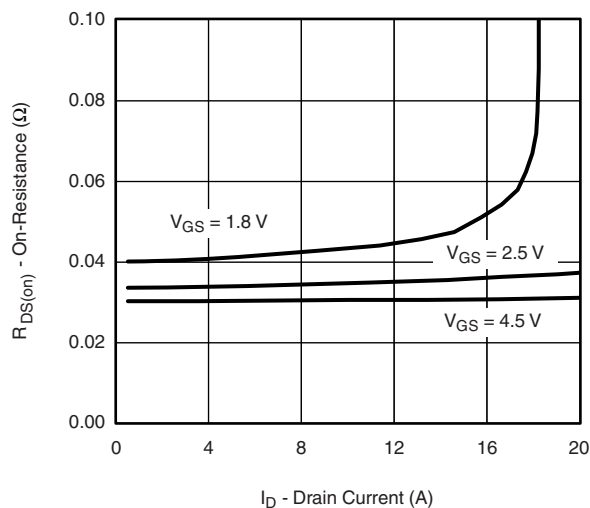
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



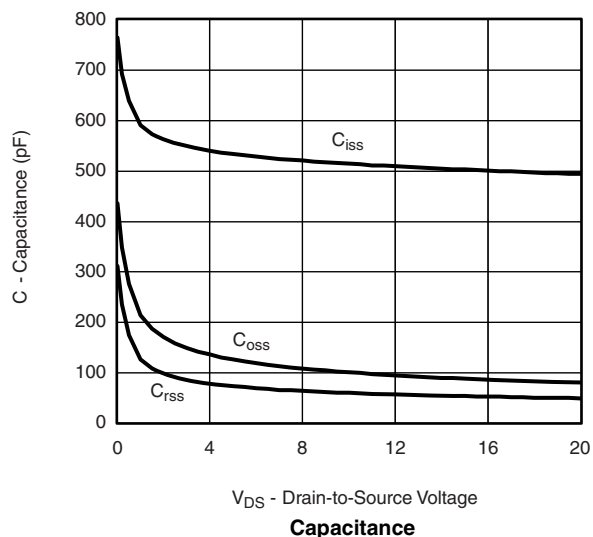
Output Characteristics



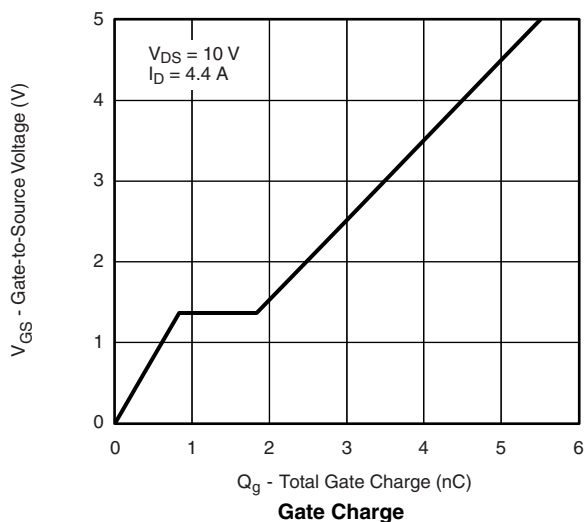
Transfer Characteristics



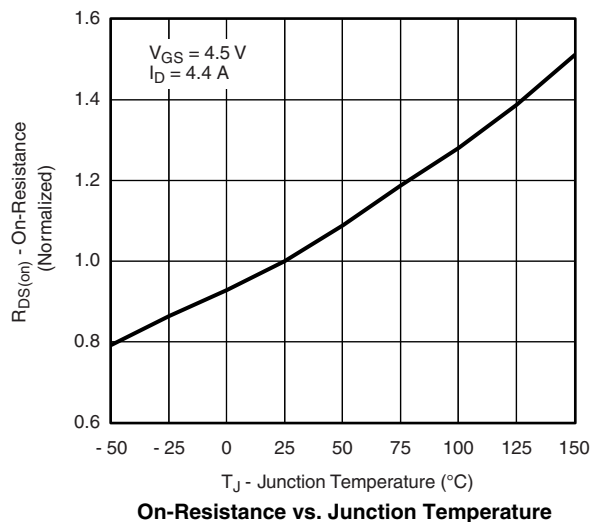
On-Resistance vs. Drain Current



Capacitance

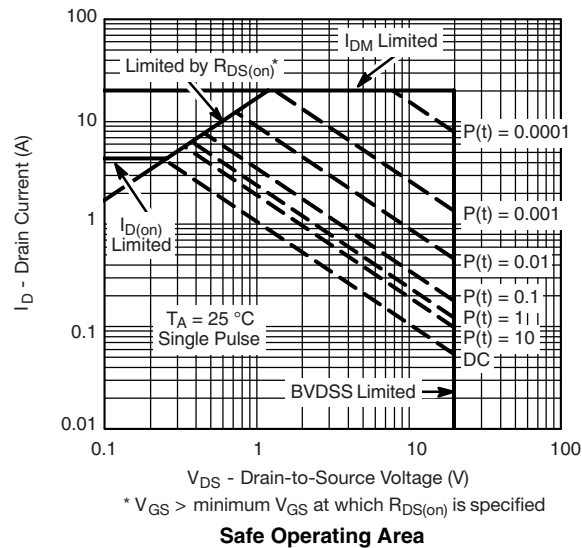
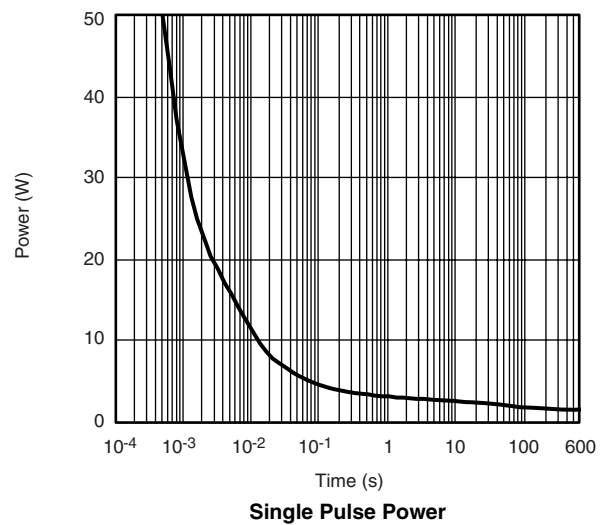
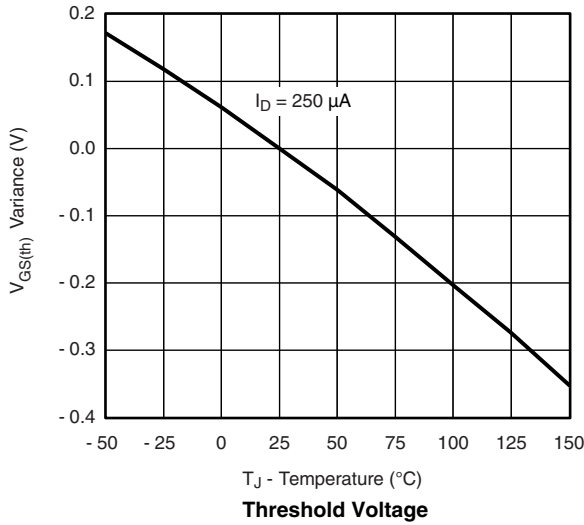
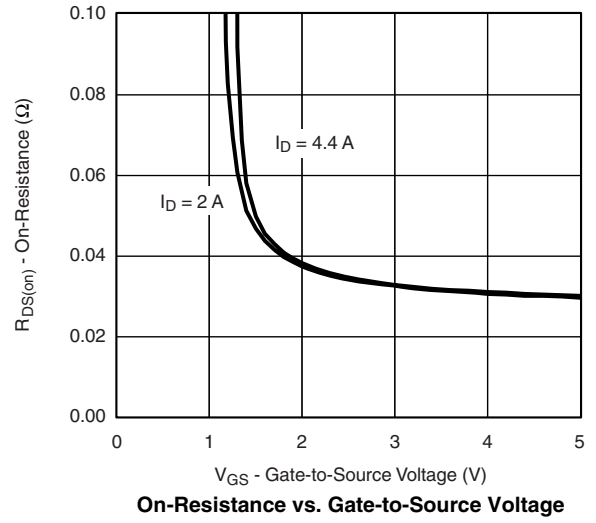
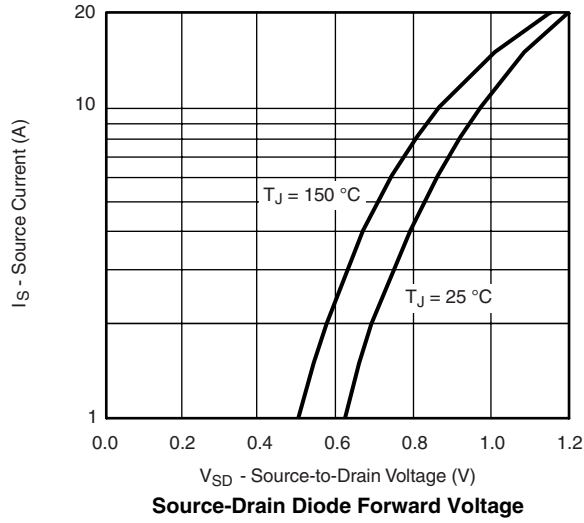


Gate Charge

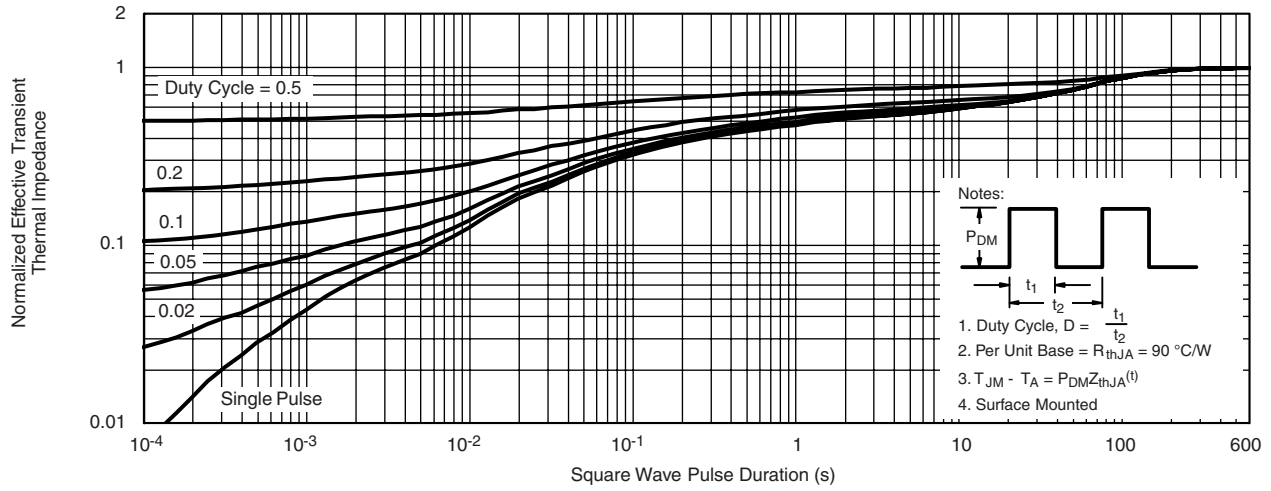


On-Resistance vs. Junction Temperature

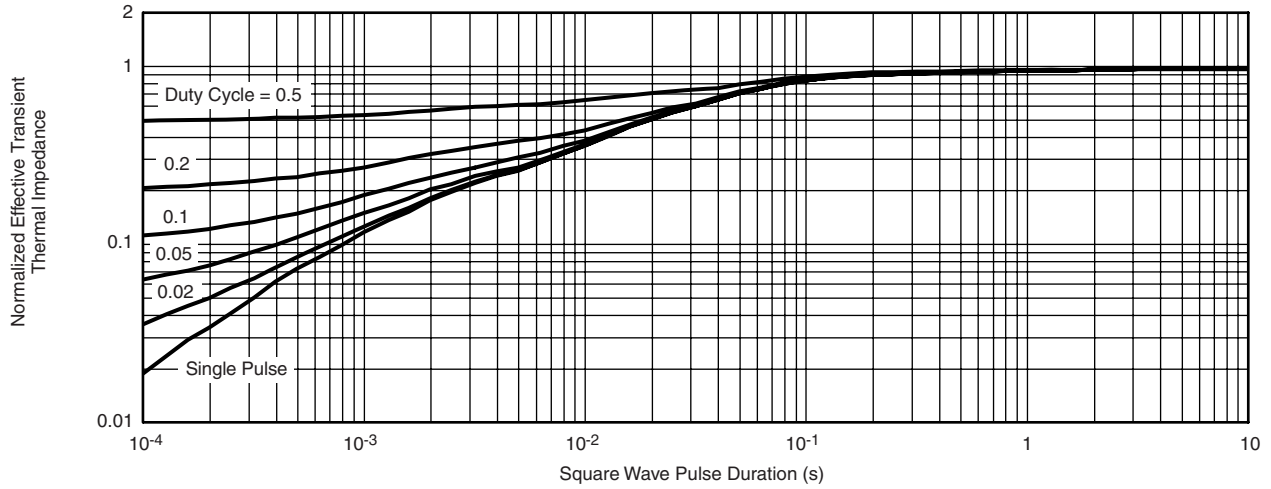
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

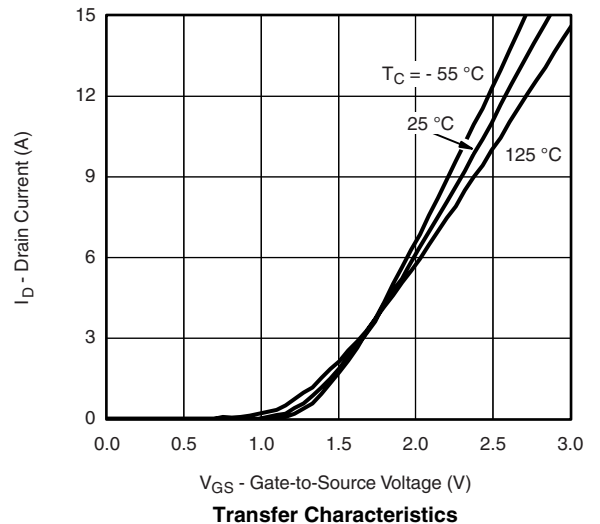
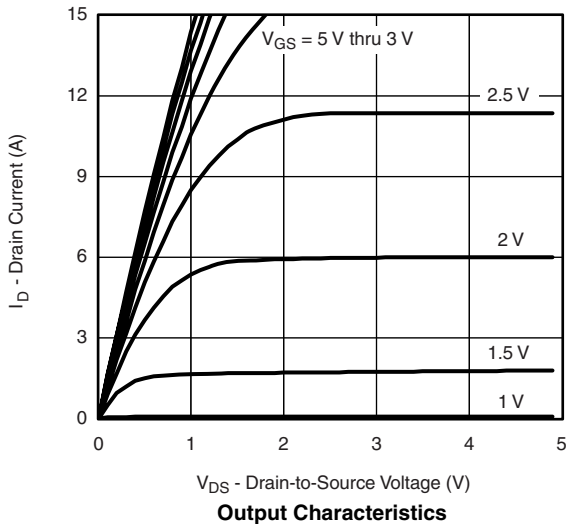


Normalized Thermal Transient Impedance, Junction-to-Ambient

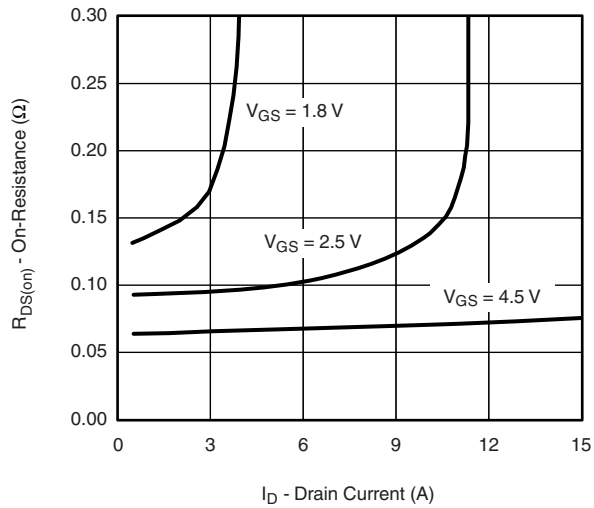


Normalized Thermal Transient Impedance, Junction-to-Foot

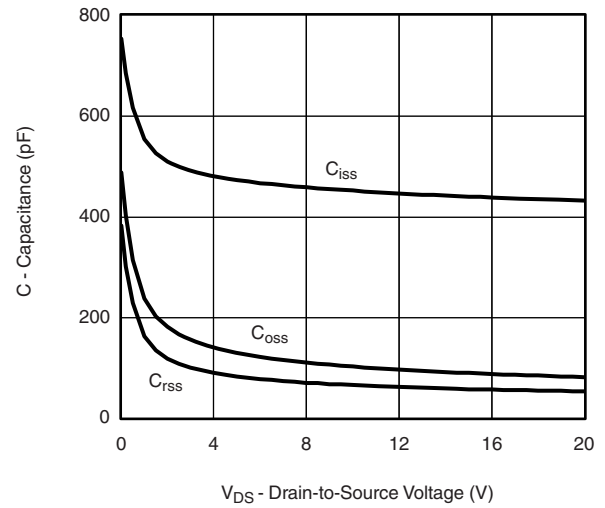
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



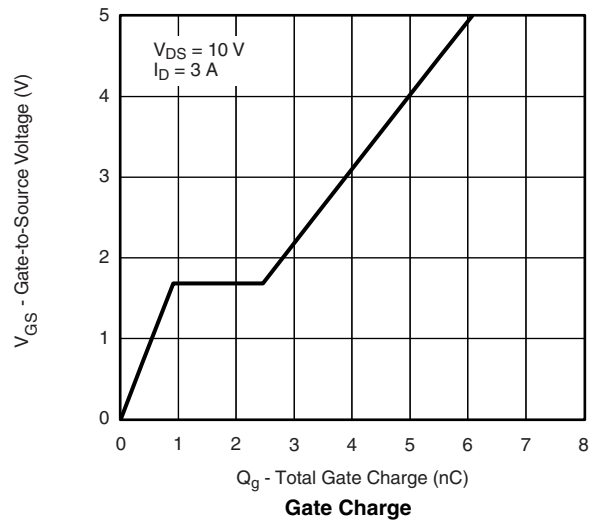
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



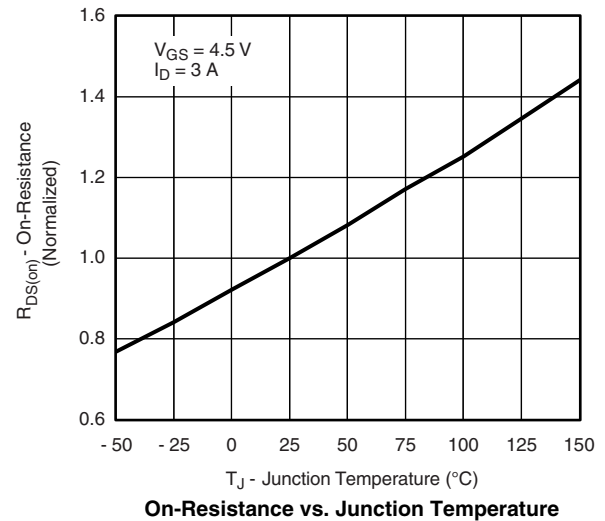
On-Resistance vs. Drain Current



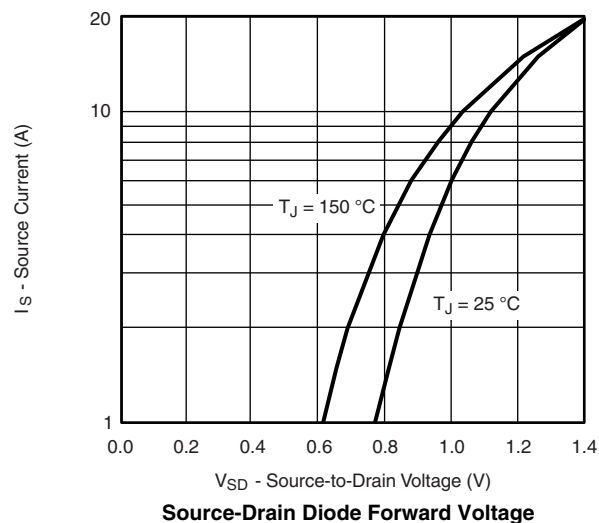
Capacitance



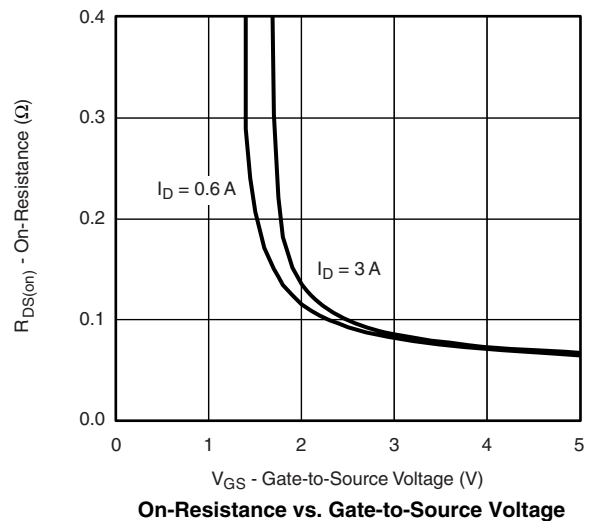
Gate Charge



On-Resistance vs. Junction Temperature

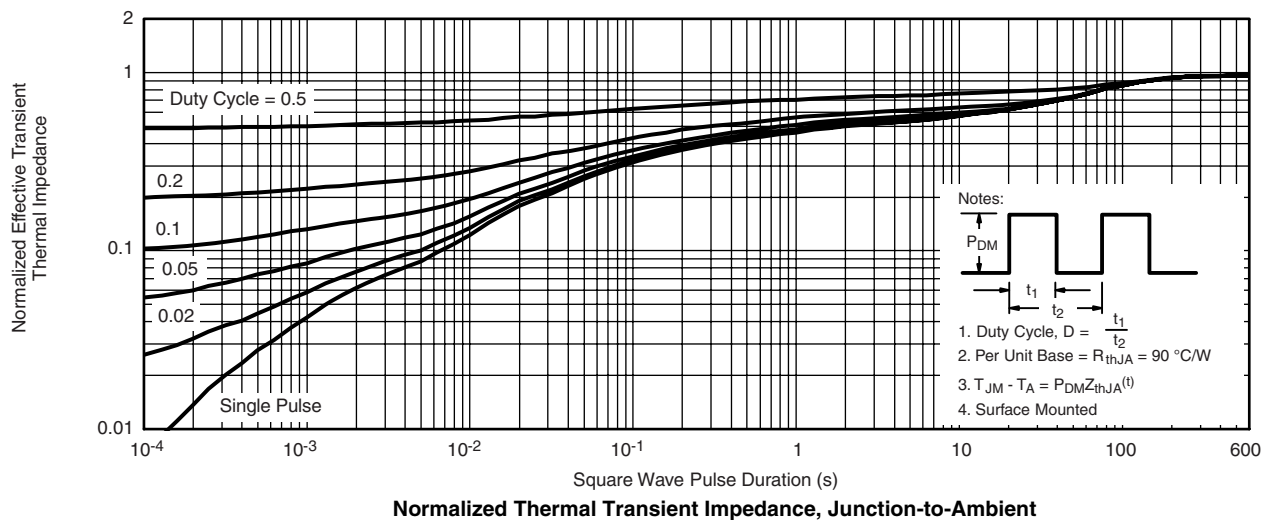
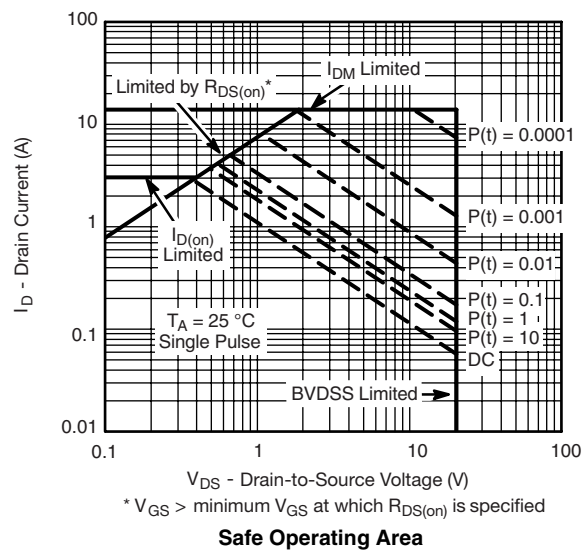
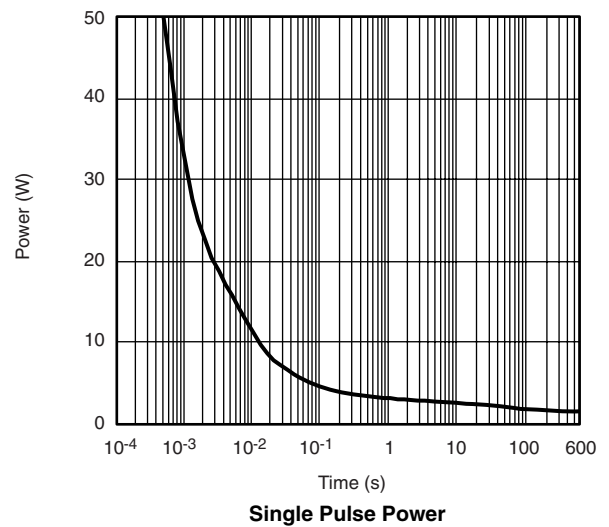
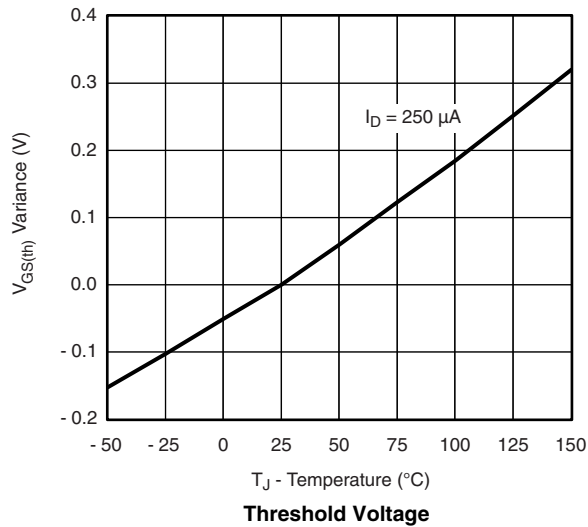


Source-Drain Diode Forward Voltage

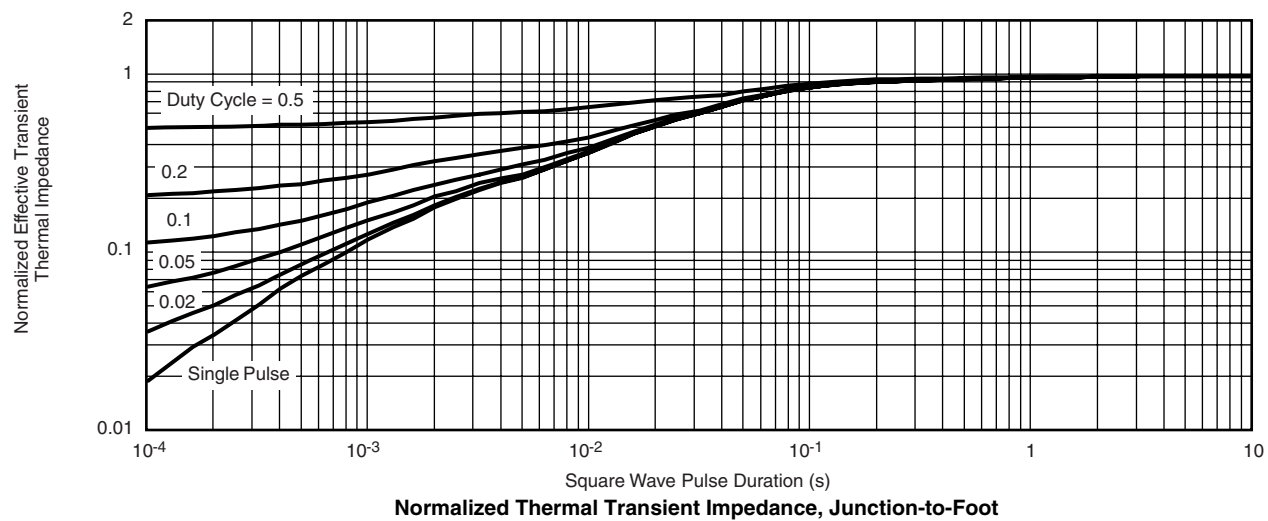


On-Resistance vs. Gate-to-Source Voltage

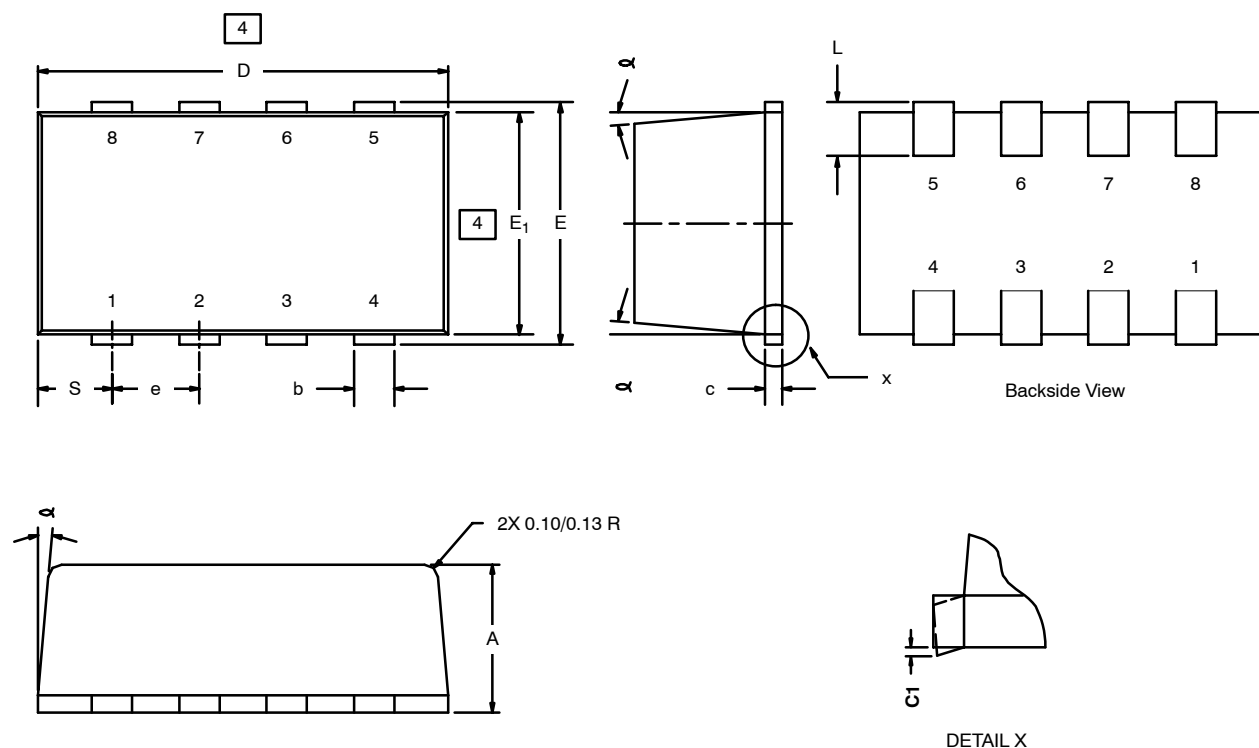
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



DFN 3x2

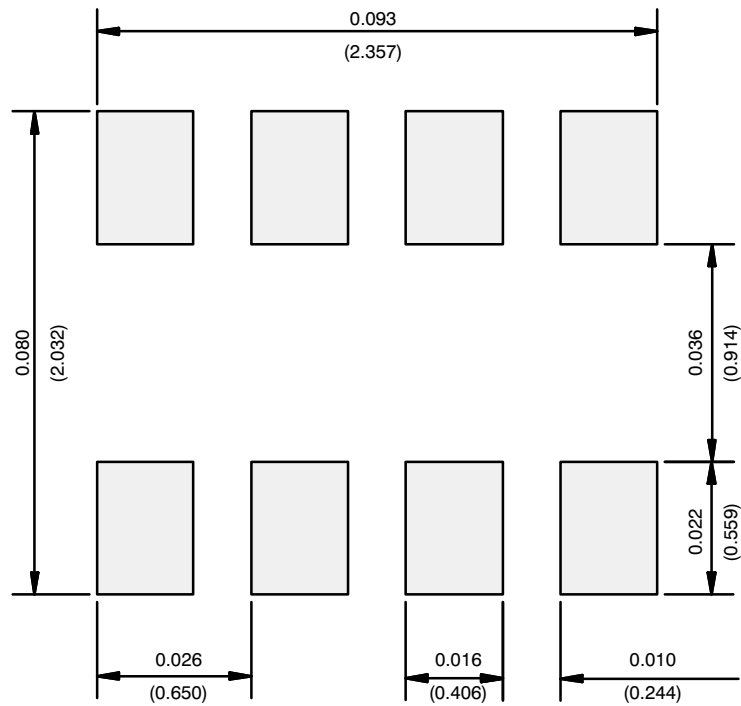


NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04 DWG: 5547						

RECOMMENDED MINIMUM PADS FOR DFN3x2



Recommended Minimum Pads
Dimensions in Inches/(mm)

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