

# TPCF8002-VB Datasheet

## N-Channel 30 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (TYP.)
30	0.016 at $V_{GS} = 10$ V	9	9 nC
	0.019 at $V_{GS} = 4.5$ V	8	

### FEATURES

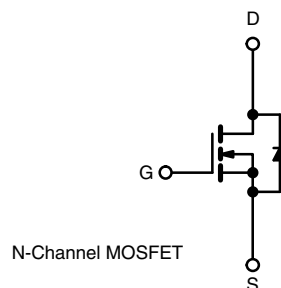
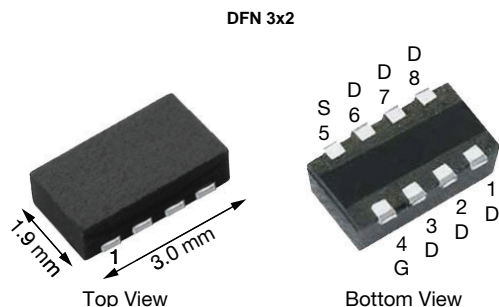
- Trench power MOSFET

### APPLICATIONS

- Load switches
- Notebook PC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	9	A
	$T_C = 70$ °C		6 <sup>a</sup>	
	$T_A = 25$ °C		6 <sup>a, b, c</sup>	
	$T_A = 70$ °C		6 <sup>a, b, c</sup>	
Pulsed Drain Current		$I_{DM}$	30	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	5.2	
	$T_A = 25$ °C		2.1 <sup>b, c</sup>	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	6.3	W
	$T_C = 70$ °C		4	
	$T_A = 25$ °C		2.5 <sup>b, c</sup>	
	$T_A = 70$ °C		1.6 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	°C
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>			260	

### THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient <sup>a, c, d</sup>	$t \leq 5$ s	$R_{thJA}$	40	50	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	15	20	

#### Notes

- Package limited,  $T_C = 25$  °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s
- Maximum under steady state conditions is 95 °C/W.
- The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

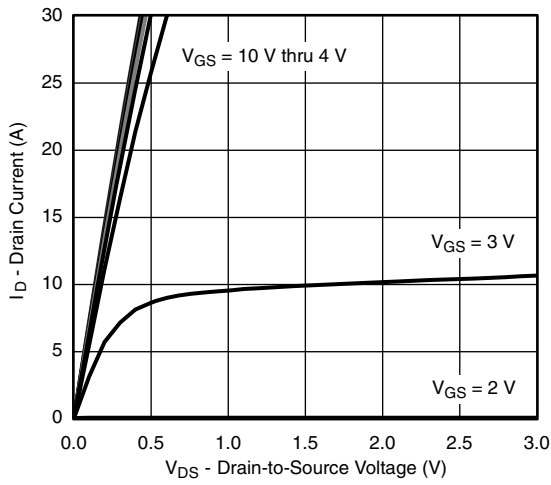
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	31	-	mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	-5.1	-	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.2	-	2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	20	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.1 A	-	0.016	-	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8.1 A	-	0.019	-	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9.1 A	-	30	-	S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	1200	-	pF
Output Capacitance	C <sub>oss</sub>		-	180	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	80	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.1 A	-	19	29	nC
		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.1 A	-	9	14	
			Gate-Source Charge	Q <sub>gs</sub>	-	
Gate-Drain Charge	Q <sub>gd</sub>	-	2.3	-		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	-	3	-	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 2.1 Ω I <sub>D</sub> ≅ 7.3 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	20	30	ns
Rise Time	t <sub>r</sub>		-	12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	20	30	
Fall Time	t <sub>f</sub>		-	10	15	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 2.1 Ω I <sub>D</sub> ≅ 7.3 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	10	15	
Rise Time	t <sub>r</sub>		-	10	15	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	20	30	
Fall Time	t <sub>f</sub>		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	5.2	A
Pulse Diode Forward Current	I <sub>SM</sub>		-	-	30	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 7.3 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 7.3 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	20	40	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>		-	11	-	ns
Reverse Recovery Rise Time	t <sub>b</sub>		-	9	-	

**Notes**

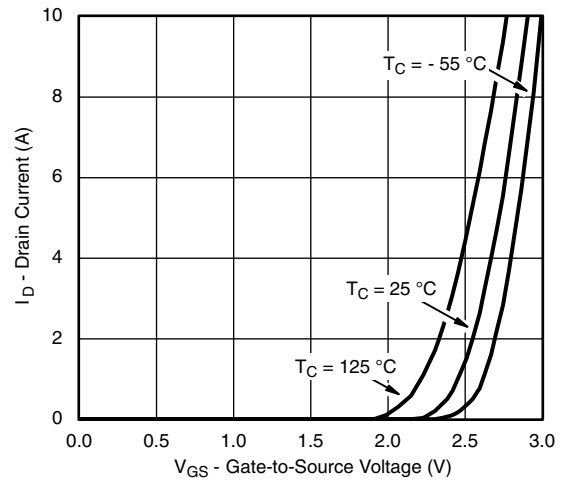
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

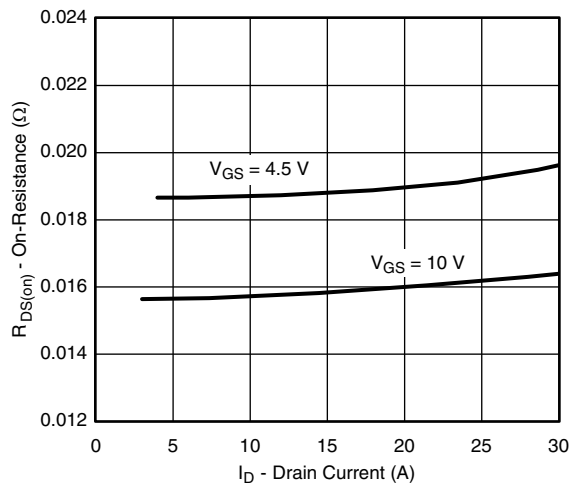
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



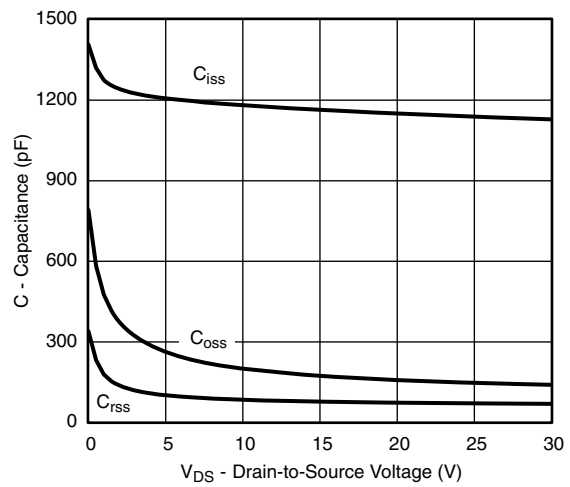
**Output Characteristics**



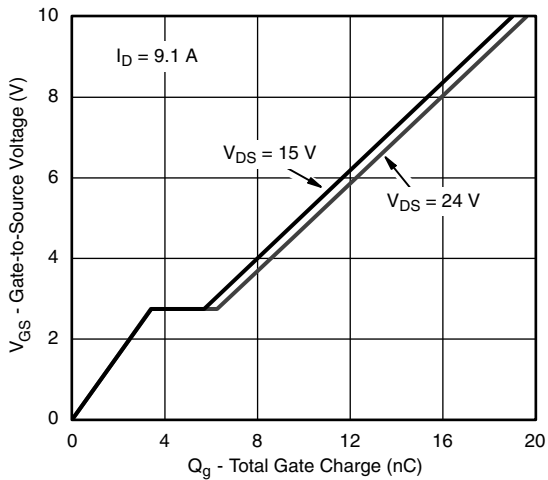
**Transfer Characteristics**



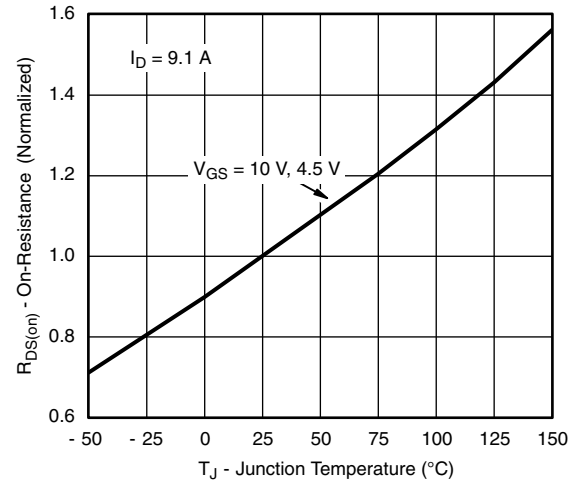
**On-Resistance vs. Drain Current**



**Capacitance**

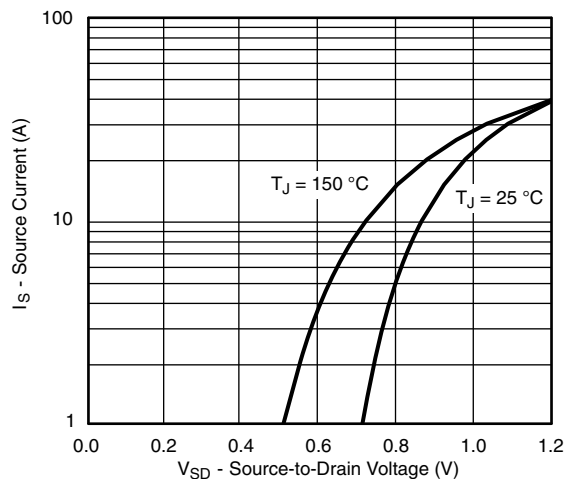


**Gate Charge**

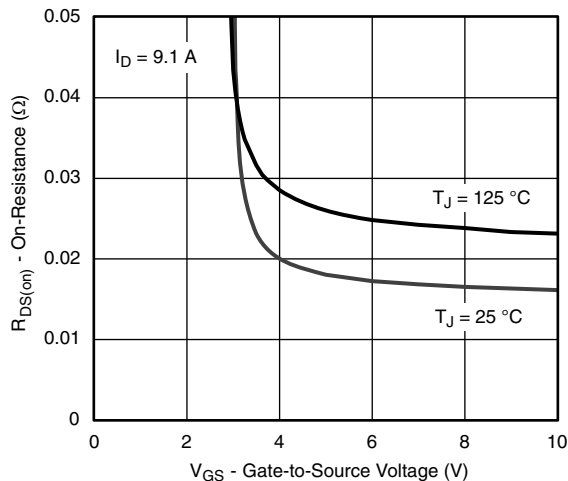


**On-Resistance vs. Junction Temperature**

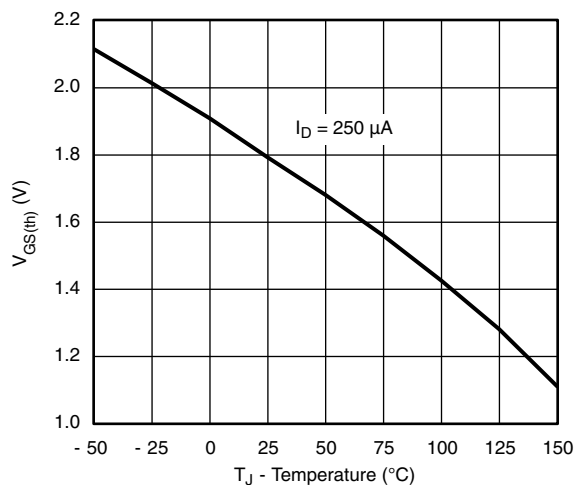
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



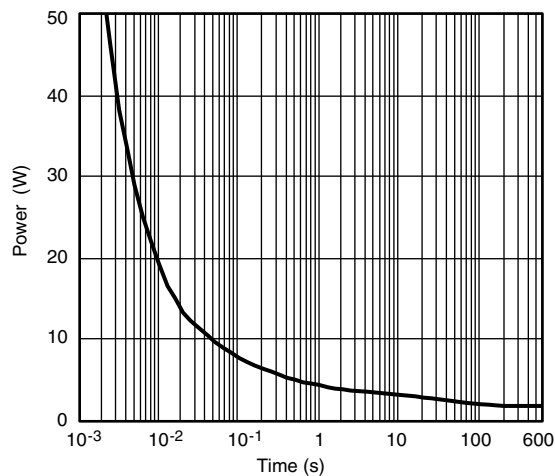
Source-Drain Diode Forward Voltage



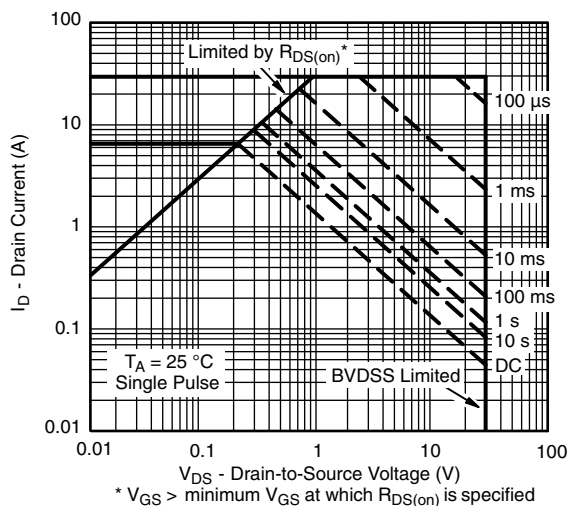
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

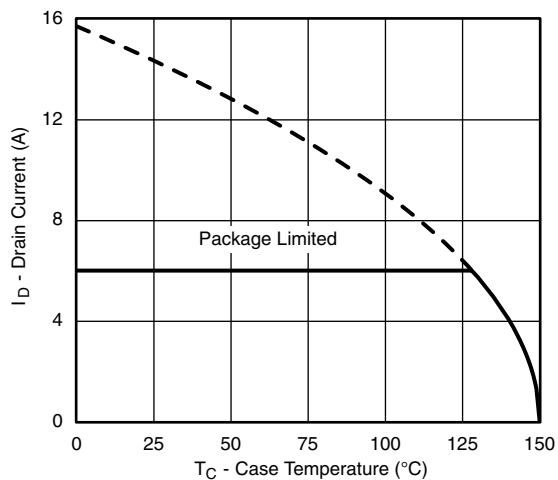


Single Pulse Power

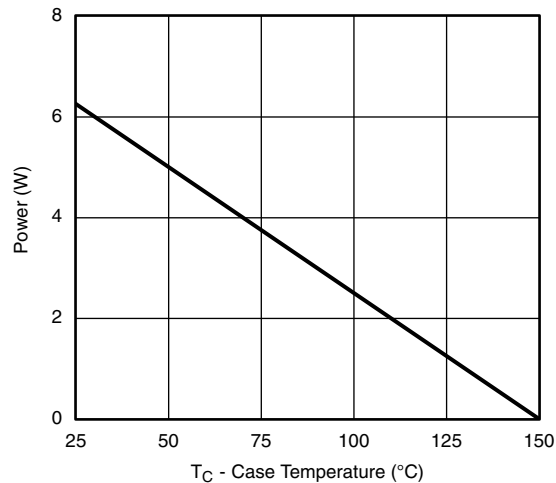


Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**

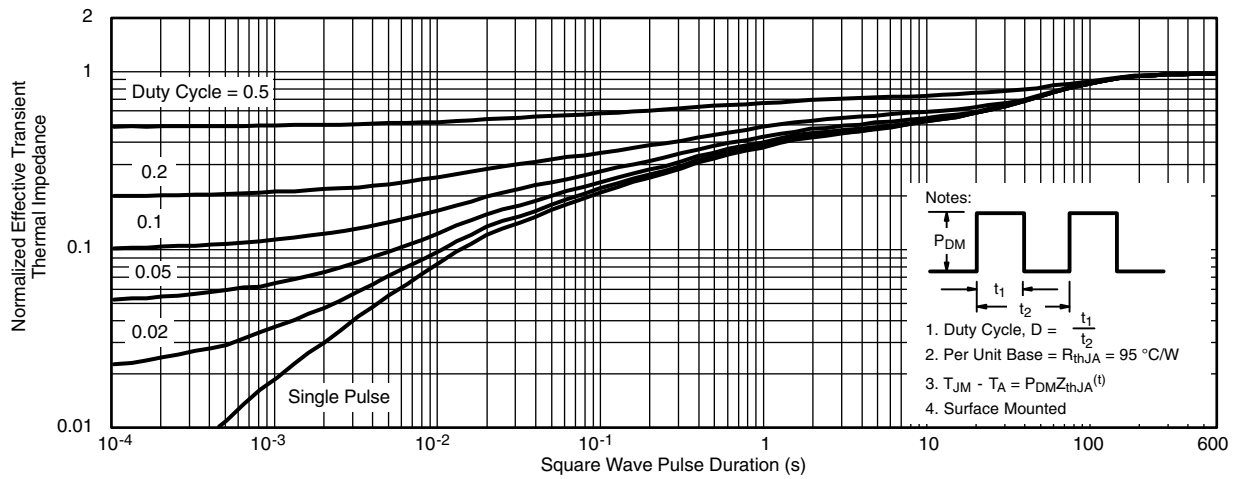


**Power Derating**

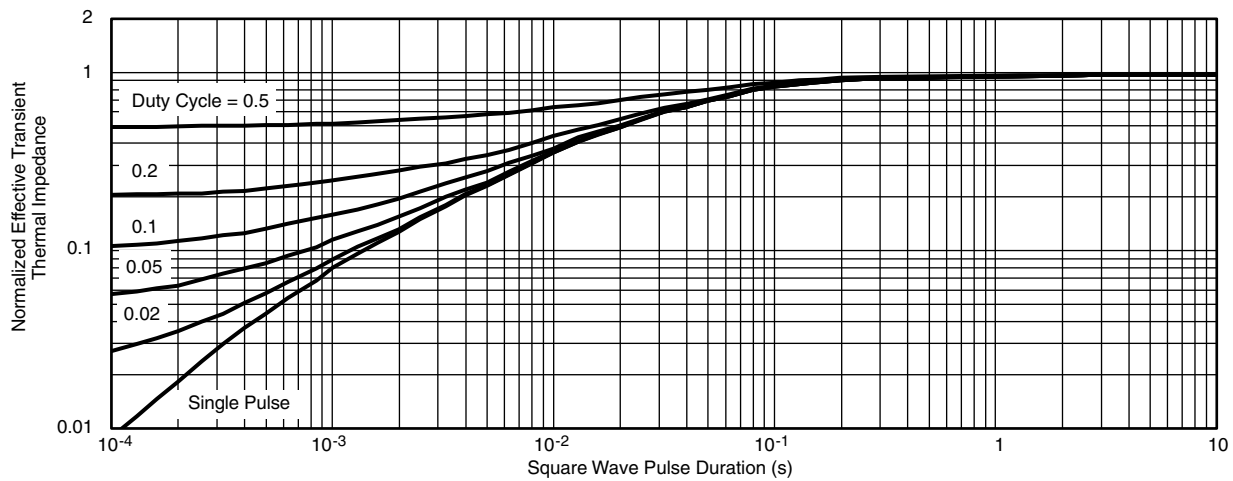
**Note**

- a. The power dissipation  $P_D$  is based on  $T_J$  (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

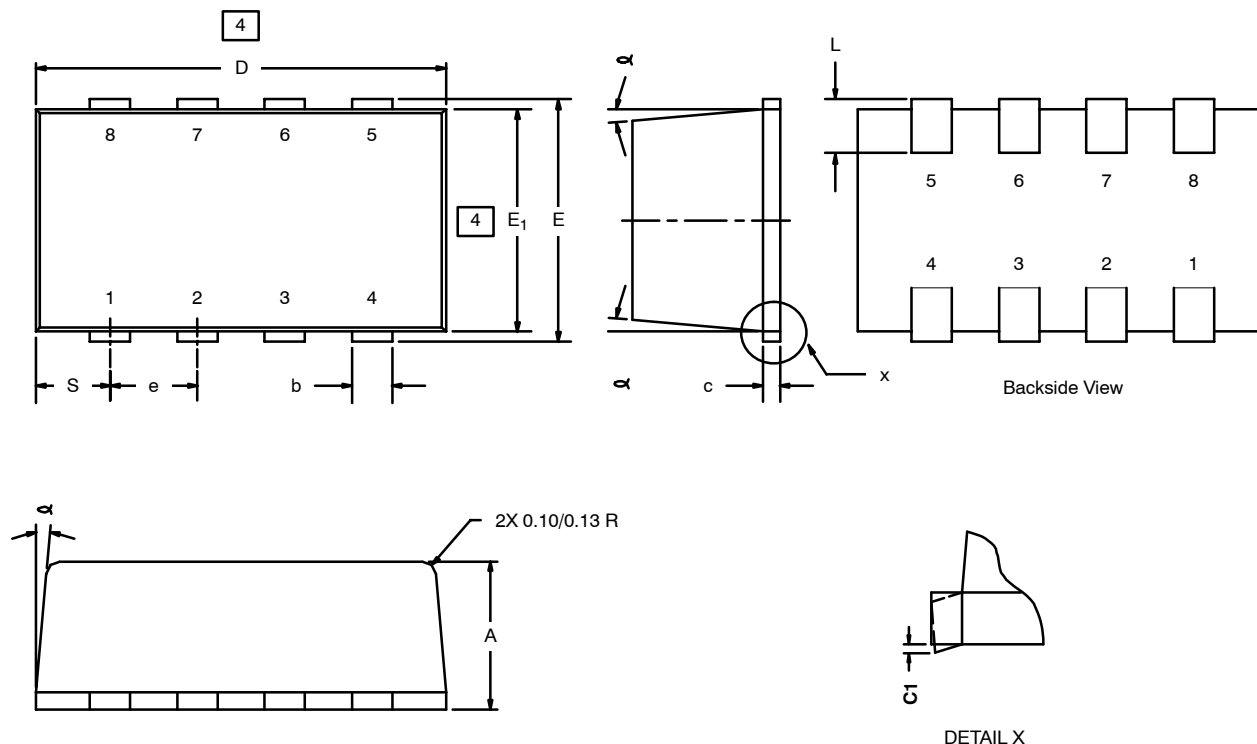


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

DFN 3x2



NOTES:

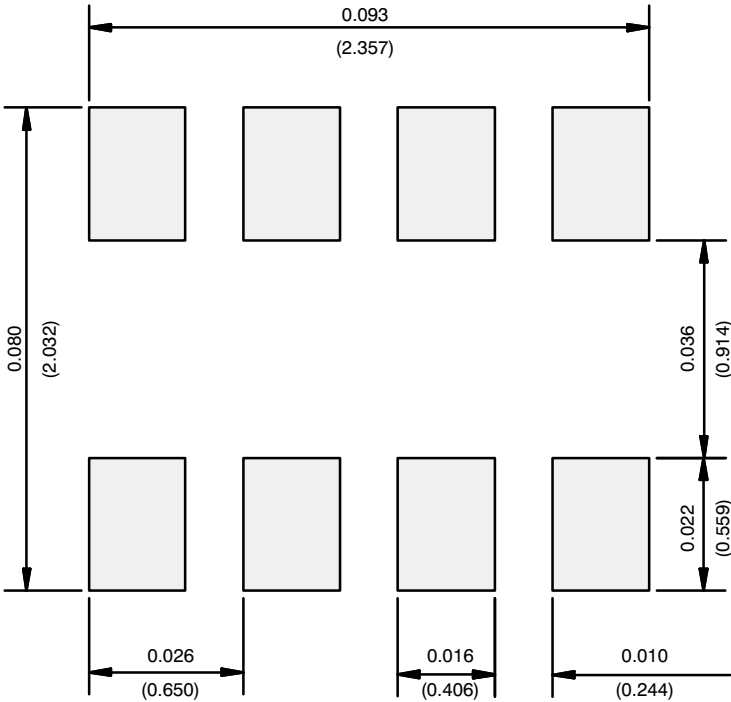
1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.

4. Dimensions exclusive of mold gate burrs.

5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04						
DWG: 5547						

RECOMMENDED MINIMUM PADS FOR DFN3x2



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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