

# SI5404BDC-T1-E3-VB Datasheet

## N-Channel 30-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.029 at $V_{GS} = 10$ V	6.7
	0.035 at $V_{GS} = 4.5$ V	6.1

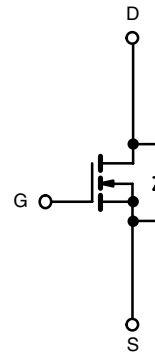
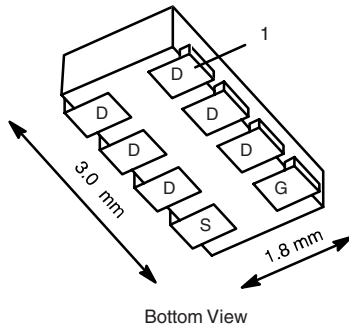
### FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- Trench Power MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

DFN 3x2



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ , unless otherwise noted<sup>1</sup>

Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	30		V
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	6.7	4.9	A
		4.8	3.5	
Pulsed Drain Current	$I_{DM}$	20		
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	2.1	1.1	
Maximum Power Dissipation <sup>a</sup>	$P_D$	2.5	1.3	W
		1.3	0.7	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>		260		

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	45	50	$^\circ\text{C/W}$
		80	95	
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	18	22	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Reliability Manual for profile. The DFN3X2 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**SPECIFICATIONS**

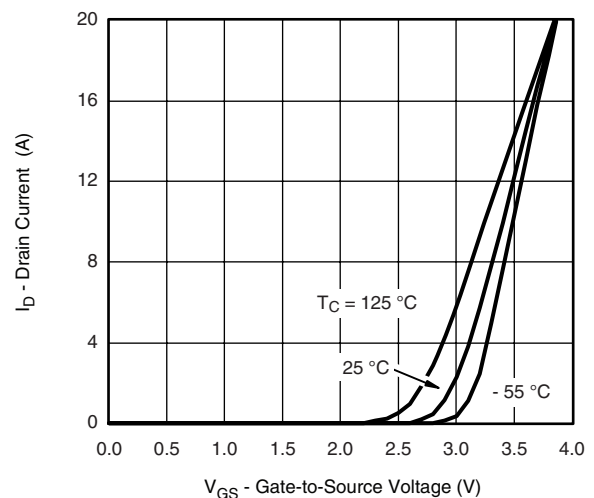
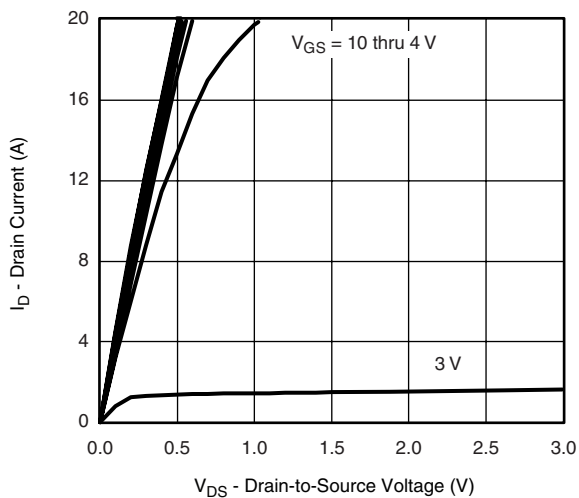
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.0		3.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30 V, V_{GS} = 0 V$			1	$\mu A$
		$V_{DS} = 30 V, V_{GS} = 0 V, T_J = 85^\circ C$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5 V, V_{GS} = 10 V$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 4.9 A$		0.029		$\Omega$
		$V_{GS} = 4.5 V, I_D = 4.4 A$		0.035		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10 V, I_D = 4.9 A$		19		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.1 A, V_{GS} = 0 V$		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 15 V, V_{GS} = 10 V, I_D = 4.9 A$		10	20	nC
Gate-Source Charge	$Q_{gs}$			1.9		
Gate-Drain Charge	$Q_{gd}$			1.6		
Gate Resistance	$R_g$	$f = 1 MHz$		14		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15 V, R_L = 15 \Omega$ $I_D \cong 1 A, V_{GEN} = 10 V, R_g = 6 \Omega$		10	15	ns
Rise Time	$t_r$			10	15	
Turn-Off Delay Time	$t_{d(off)}$			27	40	
Fall Time	$t_f$			10	15	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.1 A, di/dt = 100 A/\mu s$		20	60	

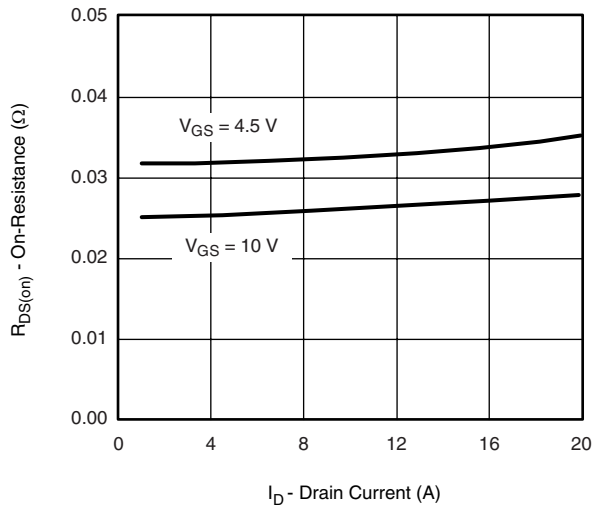
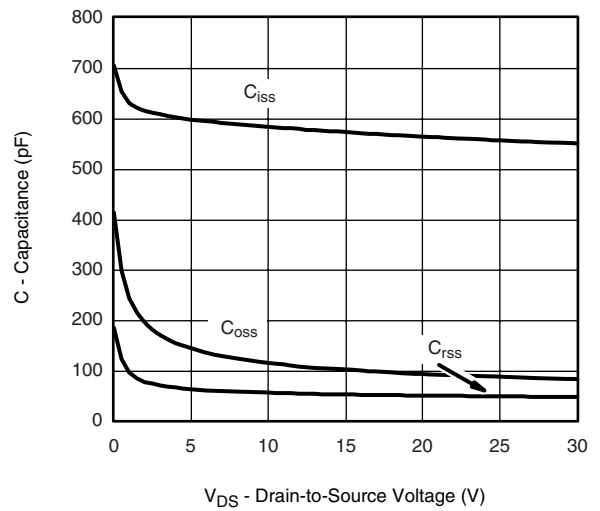
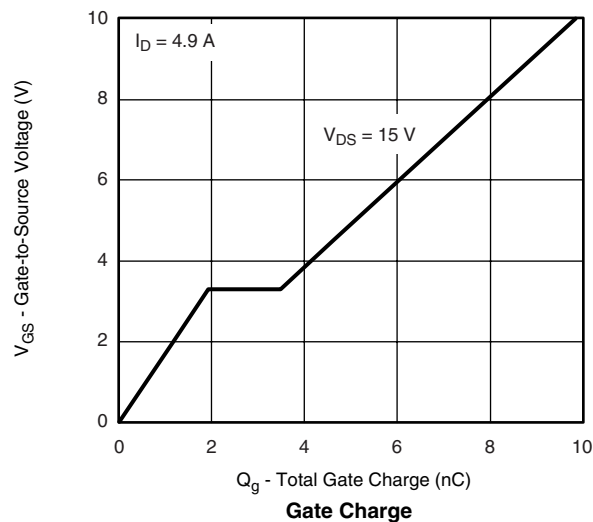
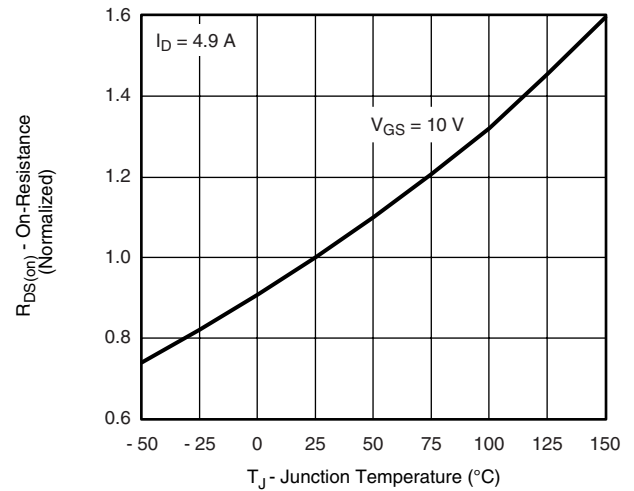
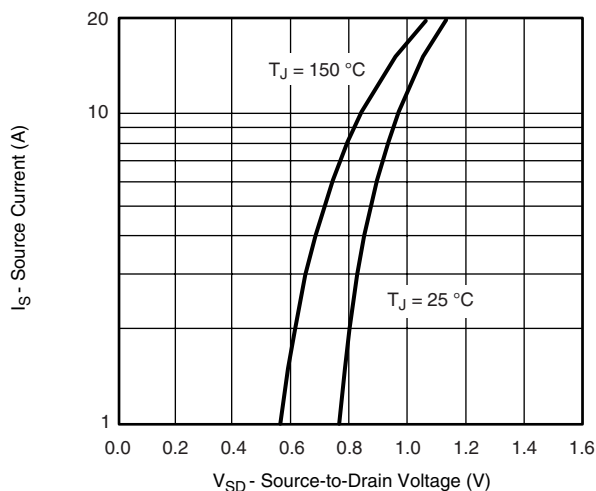
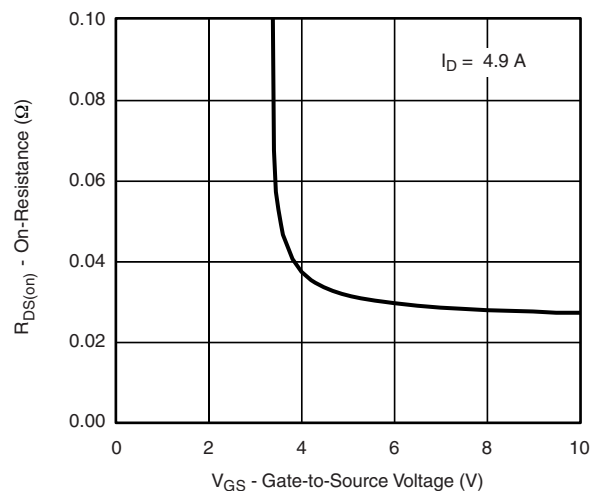
Notes:

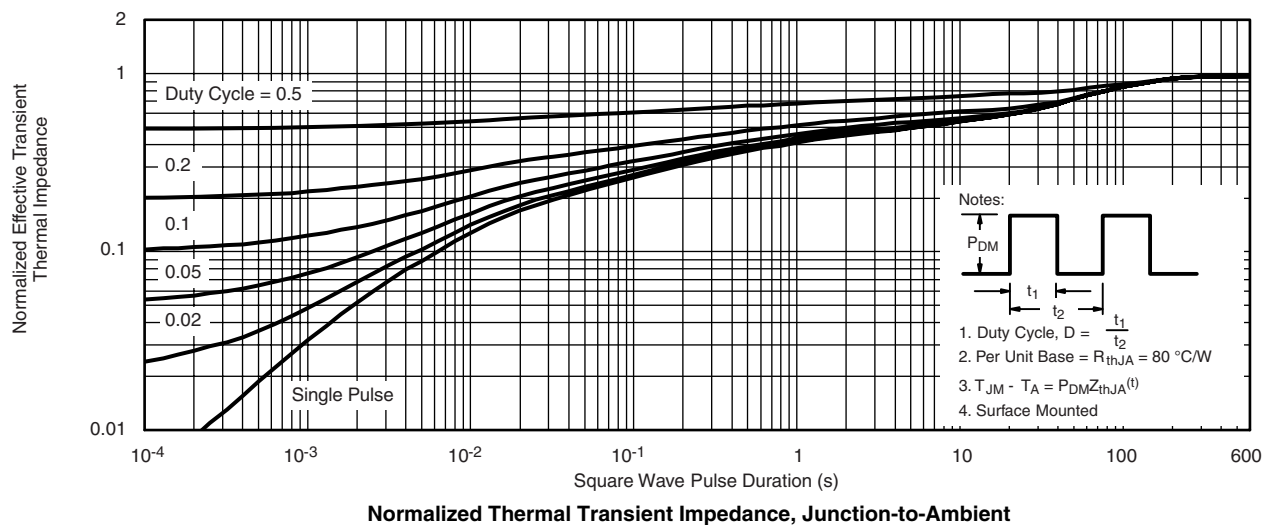
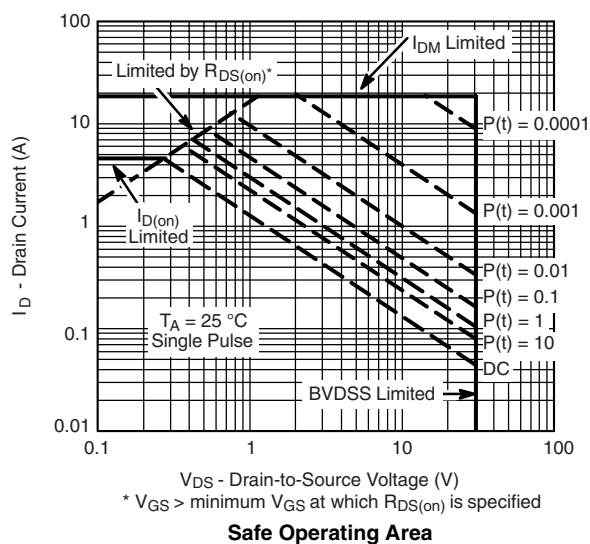
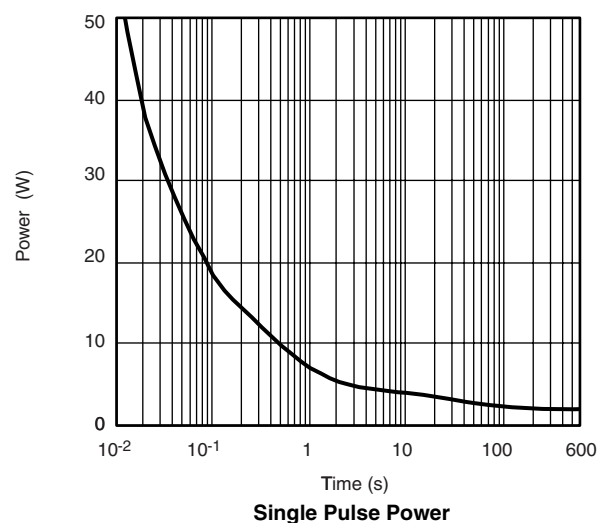
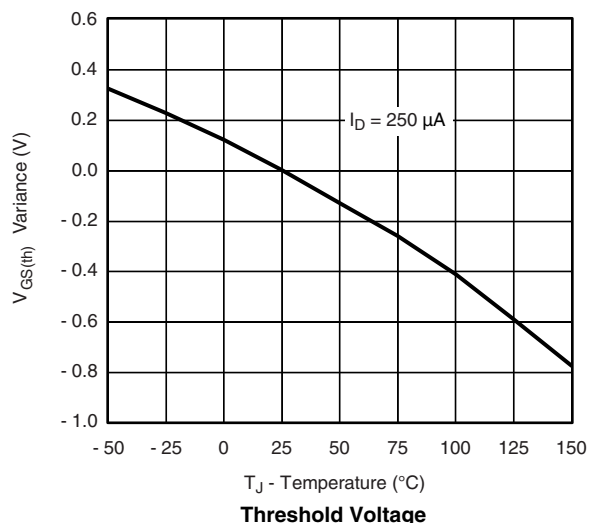
a. Pulse test; pulse width  $\leq 300 \mu s$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

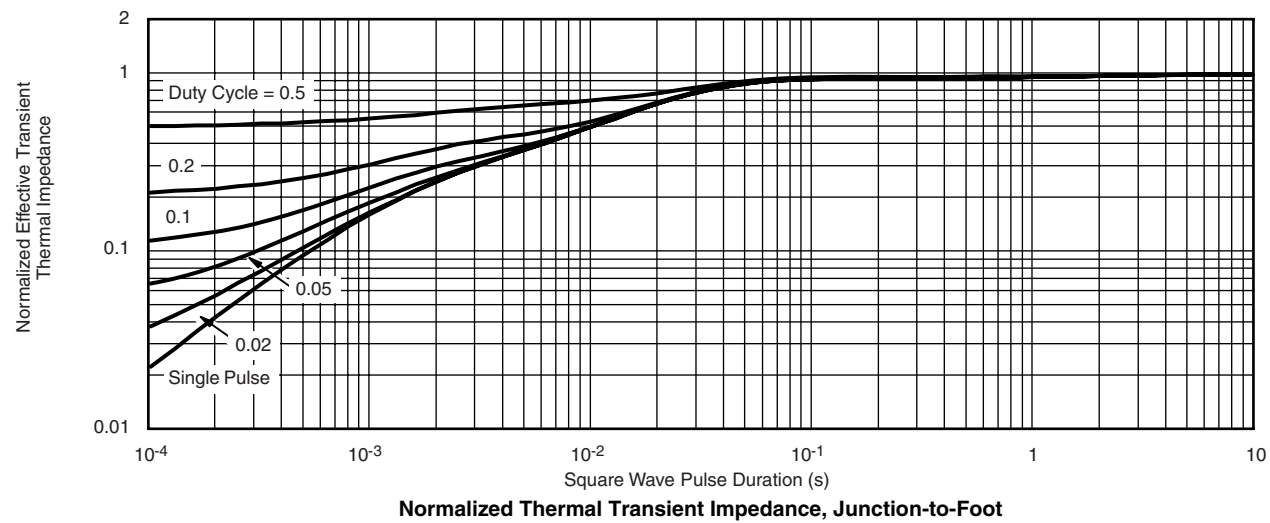
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS**  $T_J = 25^\circ C$ , unless otherwise noted

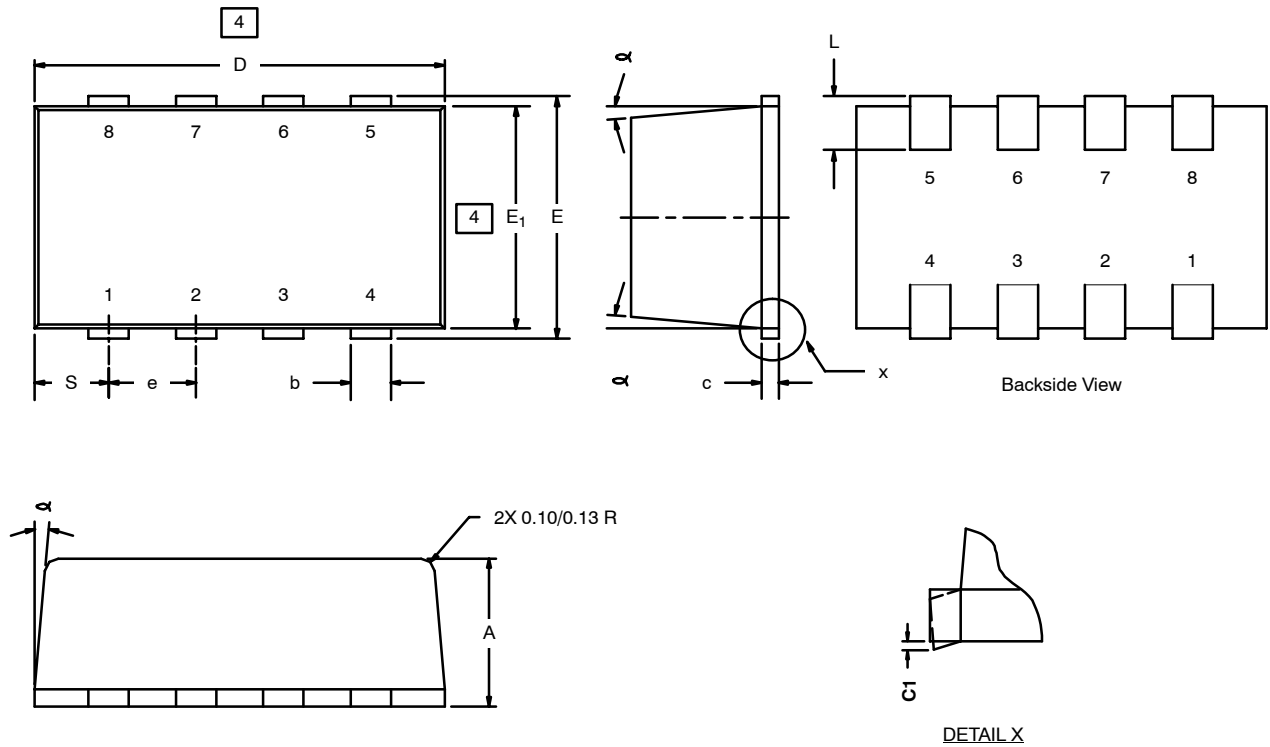
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



## DFN 3x2

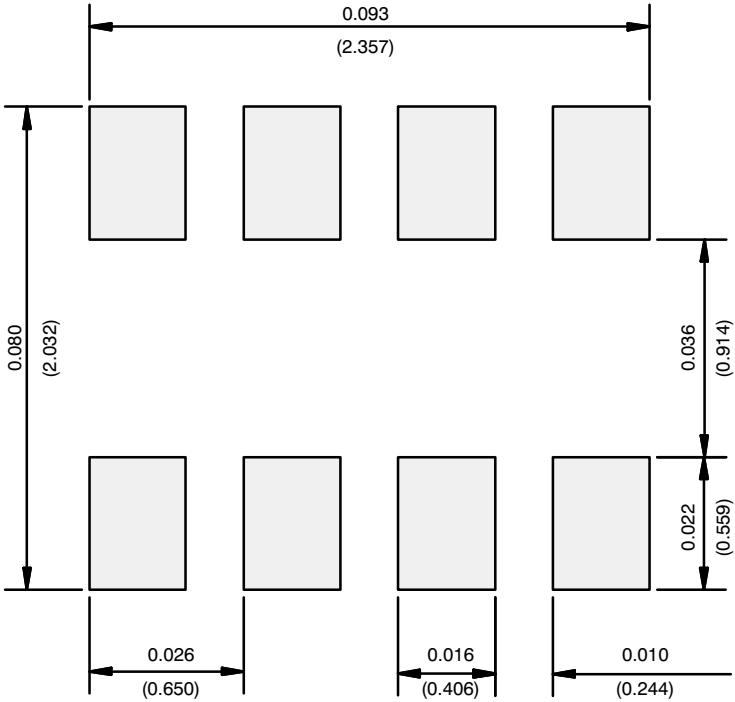


## NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04 DWG: 5547						

RECOMMENDED MINIMUM PADS FOR DFN3x2



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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