

## RT1E050RP-VB Datasheet

### P-Channel 30-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 30	0.030 at $V_{GS} = - 10$ V	- 5.1	5.1 nC
	0.042 at $V_{GS} = - 4.5$ V	- 4.1	

#### FEATURES

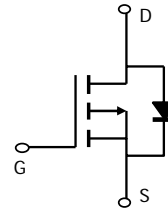
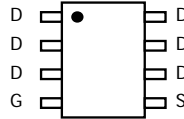
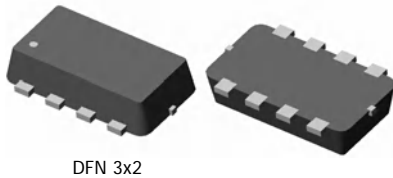
- Halogen-free According to IEC 61249-2-21 Available
- Trench Power MOSFET

#### APPLICATIONS

- Load Switch



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



#### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$ - 5.1	A
		$T_C = 70^\circ\text{C}$ - 4.1	
		$T_A = 25^\circ\text{C}$ - 4.1 <sup>b, c</sup>	
		$T_A = 70^\circ\text{C}$ - 3.3 <sup>b, c</sup>	
Pulsed Drain Current	$I_{DM}$	- 20	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$ - 2.5	
		$T_A = 25^\circ\text{C}$ - 1.67 <sup>b, c</sup>	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$ 3.0	W
		$T_C = 70^\circ\text{C}$ 2.0	
		$T_A = 25^\circ\text{C}$ 2.0 <sup>b, c</sup>	
		$T_A = 70^\circ\text{C}$ 1.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	55	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	34	41	

Notes:

- Based on  $T_C = 25^\circ\text{C}$ .
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- Maximum under Steady State conditions is 110  $^\circ\text{C/W}$ .

SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 31		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			4.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1.0		- 3.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 10 V	- 20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 4.1 A		0.030		Ω
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 1.0 A		0.042		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 4.1 A		8		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		450		pF
Output Capacitance	C <sub>oss</sub>			80		
Reverse Transfer Capacitance	C <sub>rss</sub>			63		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 4.1 A		10	15	nC
				5.1	8	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 4.1 A		1.8		
Gate-Drain Charge	Q <sub>gd</sub>			2.5		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		7		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 4.6 Ω I <sub>D</sub> ≅ - 3.3 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		40	60	ns
Rise Time	t <sub>r</sub>			80	120	
Turn-Off Delay Time	t <sub>d(off)</sub>			20	30	
Fall Time	t <sub>f</sub>			12	20	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 4.6 Ω I <sub>D</sub> ≅ - 3.3 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		5	10	
Rise Time	t <sub>r</sub>			13	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			20	30	
Fall Time	t <sub>f</sub>			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 2.5	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				- 20	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 3.3 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 3.3 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		20	30	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			20	30	nC
Reverse Recovery Fall Time	t <sub>a</sub>			14		ns
Reverse Recovery Rise Time	t <sub>b</sub>			6		

Notes:

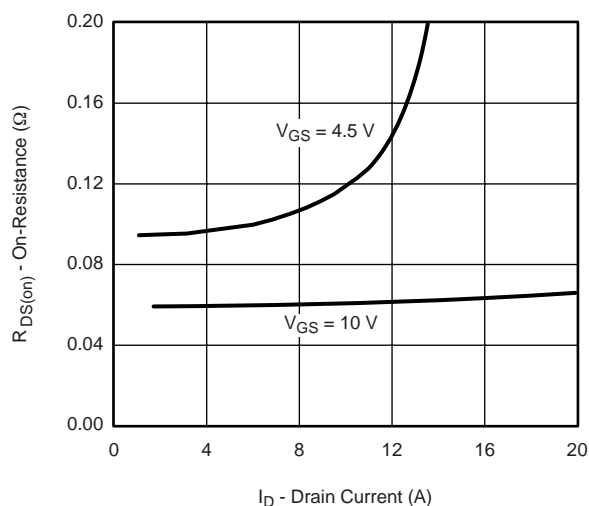
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ 

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



Source-Drain Diode Forward Voltage



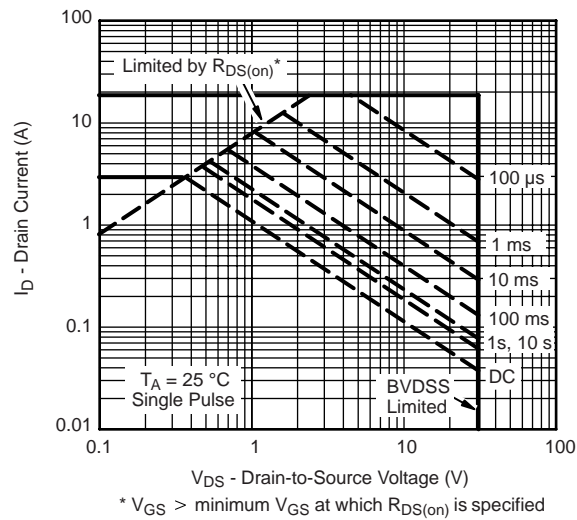
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Safe Operating Area

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



PACKAGE DIMENSIONS

ChipFET  
CASE 1206A-03  
ISSUE D



1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

- STYLE 2:
2. GATE 1
  4. GATE 2
  5. DRAIN 2
  6. DRAIN 2
  7. DRAIN 1
  8. DRAIN 1

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