

ECH8663R-VB Datasheet

Dual N-Channel 20 V (D-S) MOSFET

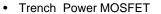
PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)			
20	0.017 at V _{GS} = 4.5 V	4.8	1.8 nC			
20	0.023 at V _{GS} = 2.5 V	3.3	1.6 110			

1206-8 Chip (Dual) D₁ S₁ D₂ D₂ D₃ D₃ D₄ D₂ D₂ D₃ D₄ D₇ D₇ D₈ D₇ D₈ D₇ D₈ D₇ D₈ D₈ D₈ D₉ D₉

Bottom View

FEATURES

 Halogen-free According to IEC 61249-2-21 Definition



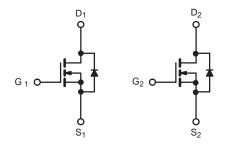
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Load Switch for Portable Applications
- DC/DC Converters



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	20	V	
Gate-Source Voltage		V_{GS}	± 12	ľ	
	T _C = 25 °C		4.8		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I _D	3		
Continuous Brain Carrette (1) = 100 °C)	T _A = 25 °C	'D	3.4 ^{b, c}		
	T _A = 70 °C		2.7 ^{b, c}	Α	
Pulsed Drain Current		I _{DM}	15		
	$T_C = 25 ^{\circ}C$		1.17		
Continuous Source-Drain Diode Current	T _A = 25 °C	IS	0.95 ^{b, c}]	
	$T_C = 25 ^{\circ}C$		1.4	 [
Maximum Power Dissipation	$T_C = 70 ^{\circ}C$	P _D	0.9	W	
Maximum Fower Dissipation	T _A = 25 °C	٠ ٦	1.14 ^{b, c}	, vv	
	T _A = 70 °C		0.73 ^{b, c}]	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 s	R_{thJA}	93	110	°C/W	
Maximum Junction-to-Foot	Steady State	$R_{th,IF}$	75	90	7 0/11	

Notes:

- a. $T_C = 25 \,^{\circ}C$.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. Maximum under steady state conditions is 150 °C/W.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static						•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V, I}_{D} = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Vns/Tu		29		m\//°(
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$		- 4		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.2		2.2	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Oata Vallana Basis Oamad	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			Α	
_	_	$V_{GS} = 4.5 \text{ V}, I_D = 3.4 \text{ A}$		0.017			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 3.0 \text{ A}$		0.023		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 3.4 A		10		S	
Dynamic ^b		-					
Input Capacitance	C _{iss}			235			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		45		pF	
Reverse Transfer Capacitance	C _{rss}	56		16			
·		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 3.4 A		3.7	6	nC	
Total Gate Charge	Qg	D3 / G3 / D		1.8	3		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 3.4 \text{ A}$		0.74			
Gate-Drain Charge	Q _{gd}			0.42			
Gate Resistance	R _g	f = 1 MHz	1	5	10	Ω	
Turn-On Delay Time	t _{d(on)}			10	20		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 5.6 \Omega$		15	30		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 2.7 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		10	20		
Fall Time	t _f			10	20		
Turn-On Delay Time	t _{d(on)}			5	10	ns	
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_1 = 5.6 \Omega$		15	30		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 2.7 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		10	20		
Fall Time	t _f			10	20		
Drain-Source Body Diode Characteristic	ss ·					l	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			1.17		
Pulse Diode Forward Current	I _{SM}				15	A	
Body Diode Voltage	V _{SD}	$I_S = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.85	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			10	20	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			4	10	nC	
Reverse Recovery Fall Time	t _a	$I_F = 2.7 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		6			
Reverse Recovery Rise Time	t _b	\dashv		4		ns	

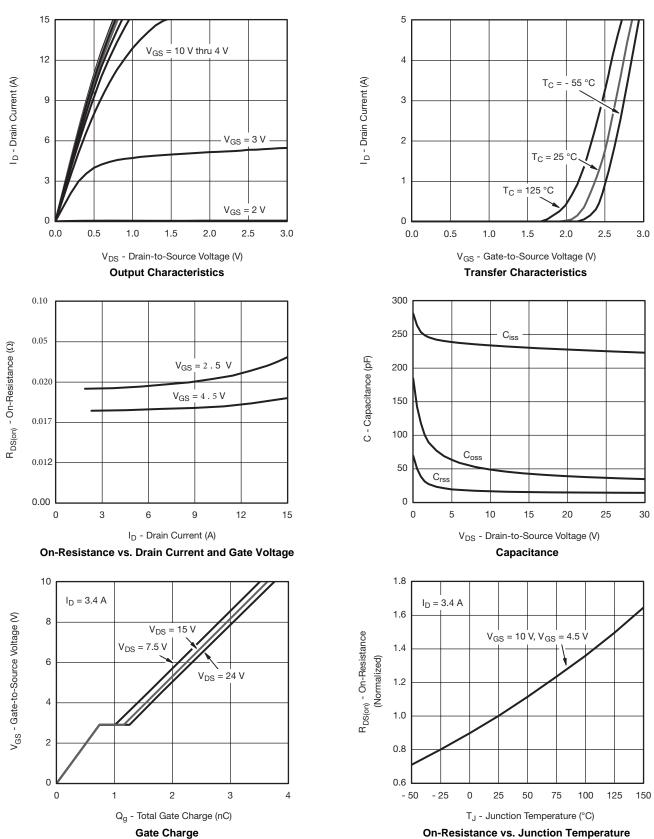
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

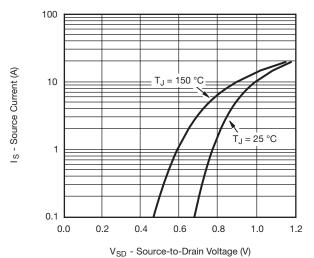
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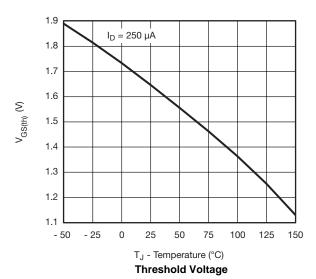


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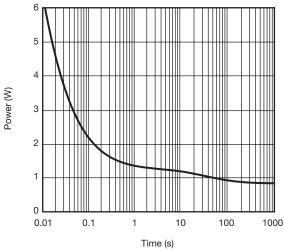


Source-Drain Diode Forward Voltage

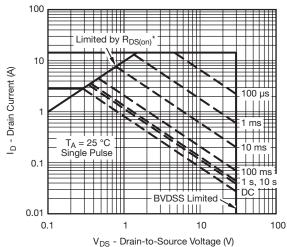


0.14 $I_D = 3.4 A$ 0.12 R_{DS(on)} - On-Resistance (Ω) 0.10 T_J = 125 °C 0.08 0.06 $T_J = 25 \, ^{\circ}C$ 0.04 0.02 0.00 0 8 10 V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



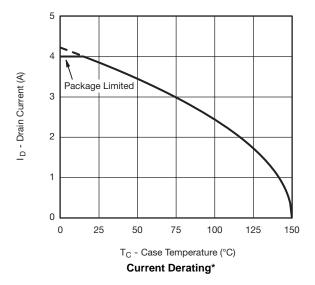
Single Pulse Power (Junction-to-Ambient)

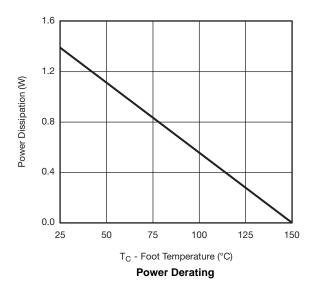


* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

Safe Operating Area, Junction-to-Ambient



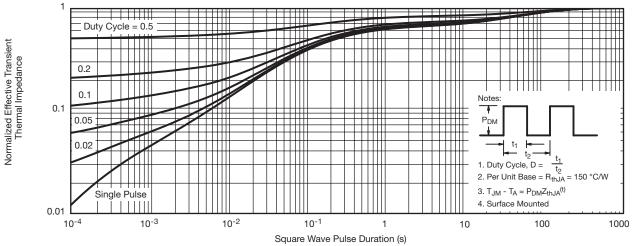




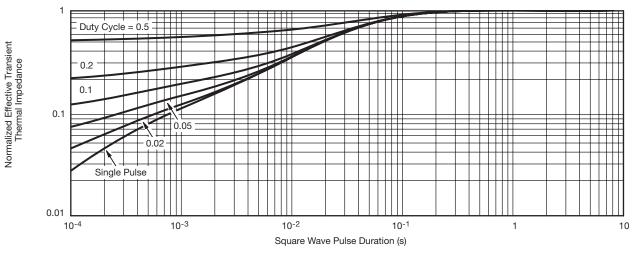
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^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

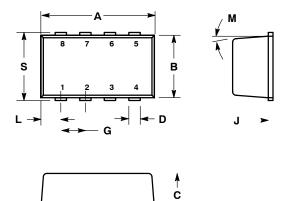


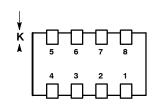
Normalized Thermal Transient Impedance, Junction-to-Foot



PACKAGE DIMENSIONS

ChipFET CASE 1206A-03 ISSUE D





STYLE 2:

- 2. GATE 1
- 4. GATE 2

- 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
 LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
 DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
 NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

	MILLIMETERS		INC	INCHES	
DIM	MIN	MAX	MIN	MAX	
Α	2.95	3.10	0.116	0.122	
В	1.55	1.70	0.061	0.067	
C	1.00	1.10	0.039	0.043	
D	0.25	0.35	0.010	0.014	
G	0.65 BSC		0.02	5 BSC	
J	0.10	0.20	0.004	0.008	
K	0.28	0.42	0.011	0.017	
L	0.55 BSC		0.02	2 BSC	
M	5° NOM		5 °	NOM	
S	1.80	2.00	0.072	0.080	



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