

## SiA429DJT-T1-GE3-VB Datasheet

### P-Channel 20 V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
- 20	0.030 at $V_{GS} = -4.5$ V	$-10^a$	18 nC
	0.040 at $V_{GS} = -2.5$ V	$-g^a$	

#### FEATURES

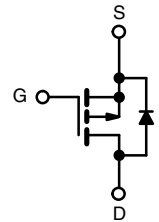
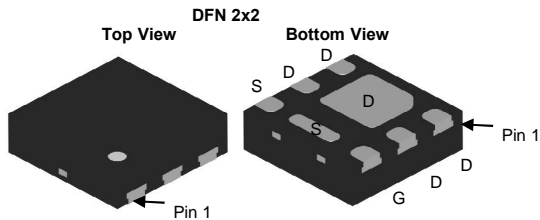
- Trench Power MOSFET
- Thermally Enhanced DFN2X2 Package
- Small Footprint Area
- Low On-Resistance



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

#### APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Devices



P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	- $10^a$
		$T_C = 70^\circ\text{C}$	- $8^a$
		$T_A = 25^\circ\text{C}$	- $10^{b,c}$
		$T_A = 70^\circ\text{C}$	- $8^{b,c}$
Pulsed Drain Current ( $t = 300 \mu\text{s}$ )	$I_{DM}$	- 30	
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	- $10^a$
		$T_A = 25^\circ\text{C}$	- $2.5^{b,c}$
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	17
		$T_C = 70^\circ\text{C}$	11
		$T_A = 25^\circ\text{C}$	$3.3^{b,c}$
		$T_A = 70^\circ\text{C}$	$2.1^{b,c}$
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		250	

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	28	38	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	5.6	7.5	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c.  $t = 5$  s.

d. See solder profile The DFN2X2 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

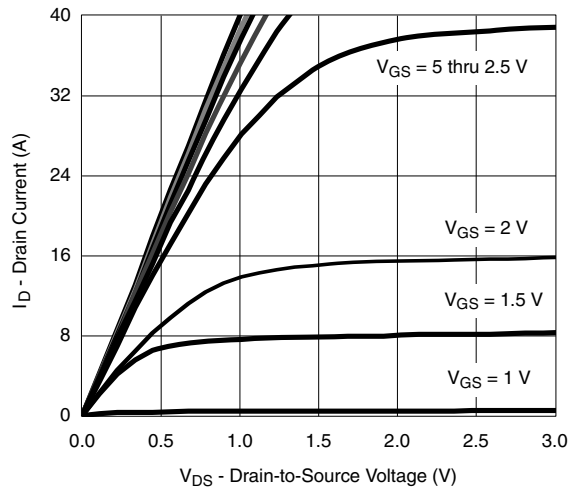
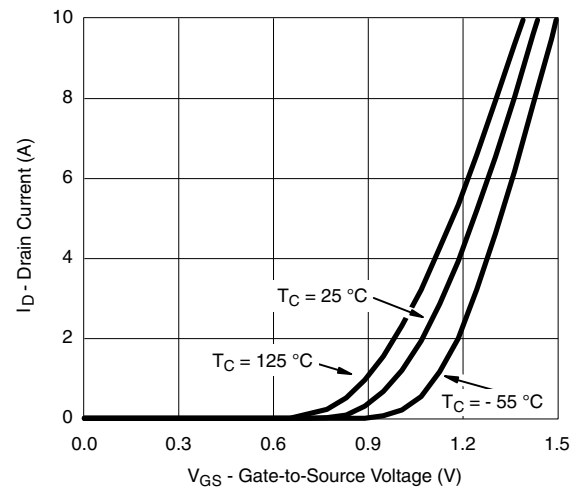
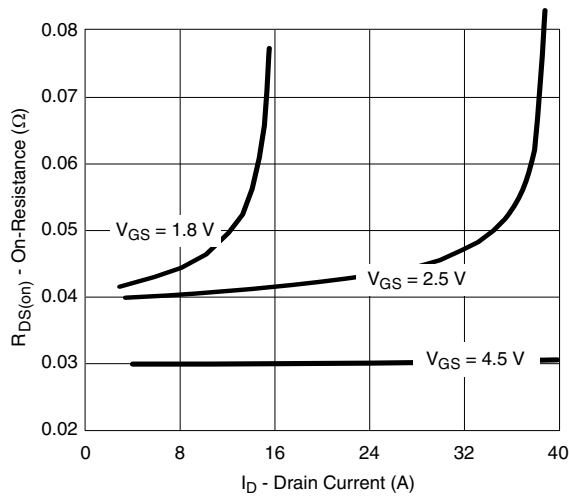
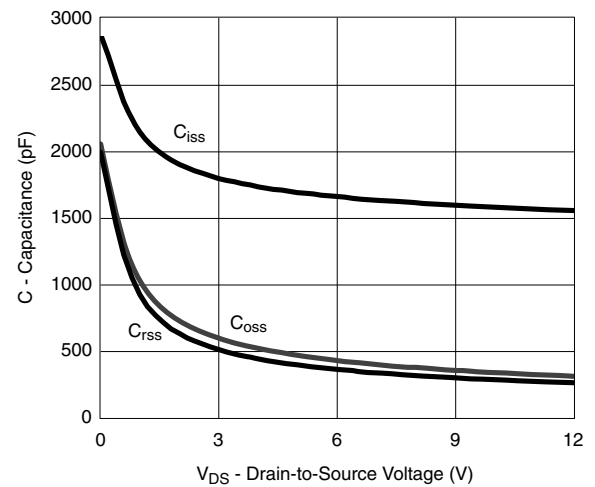
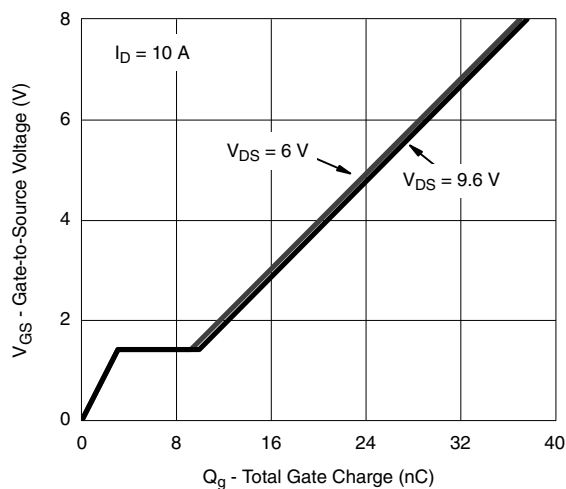
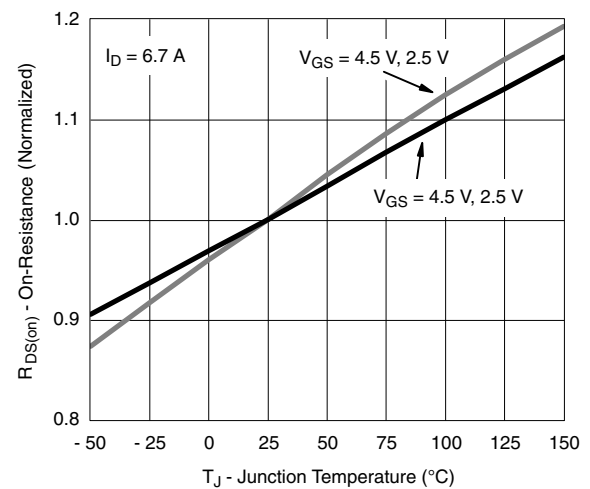
f. Maximum under steady state conditions is  $80^\circ\text{C/W}$ .

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 20			V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 11		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			2.7			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 0.4		- 1	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 12 V, V <sub>GS</sub> = 0 V			- 1	μA	
		V <sub>DS</sub> = - 12 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 4.5 V	- 20			A	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 6.7 A		0.030		Ω	
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 6.2 A		0.040			
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 2.3 A		0.042			
		V <sub>GS</sub> = - 1.5 V, I <sub>D</sub> = - 1 A		0.050			
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 6.7 A		30		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1600		pF	
Output Capacitance	C <sub>oss</sub>			430			
Reverse Transfer Capacitance	C <sub>rss</sub>			370			
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 6 V, V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 10 A		38	54	nC	
		V <sub>DS</sub> = - 6 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 10 A		23	33		
					3		
					6.5		
Gate-Source Charge	Q <sub>gs</sub>						
Gate-Drain Charge	Q <sub>gd</sub>						
Gate Resistance	R <sub>g</sub>	f = 1 MHz		7		Ω	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 6 V, R <sub>L</sub> = 0.75 Ω I <sub>D</sub> ≅ - 8 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		20	30	ns	
Rise Time	t <sub>r</sub>			40	60		
Turn-Off Delay Time	t <sub>d(off)</sub>			65	100		
Fall Time	t <sub>f</sub>			40	60		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 6 V, R <sub>L</sub> = 0.75 Ω I <sub>D</sub> ≅ - 8 A, V <sub>GEN</sub> = - 8 V, R <sub>g</sub> = 1 Ω		10	15		
Rise Time	t <sub>r</sub>			12	20		
Turn-Off Delay Time	t <sub>d(off)</sub>			70	105		
Fall Time	t <sub>f</sub>			40	60		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 10	A	
Pulse Diode Forward Current	I <sub>SM</sub>				30		
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 8 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 8 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		40	60	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			20	30	nC	
Reverse Recovery Fall Time	t <sub>a</sub>			14		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			26			

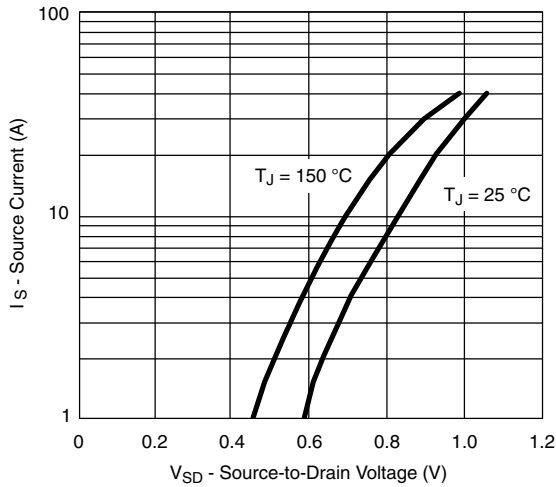
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

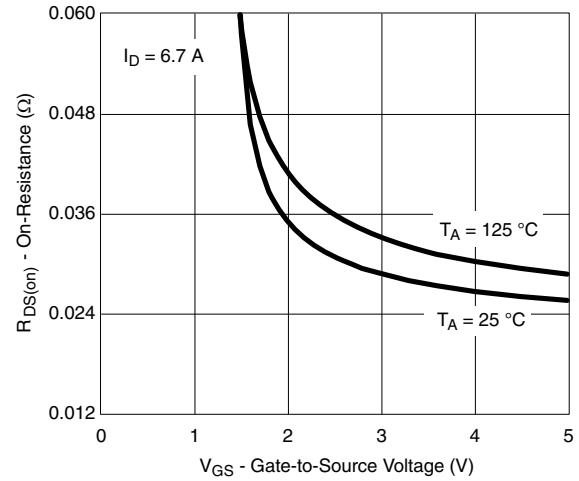
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

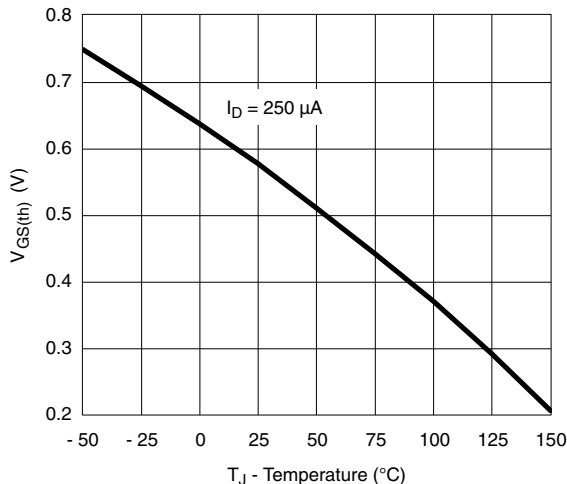
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



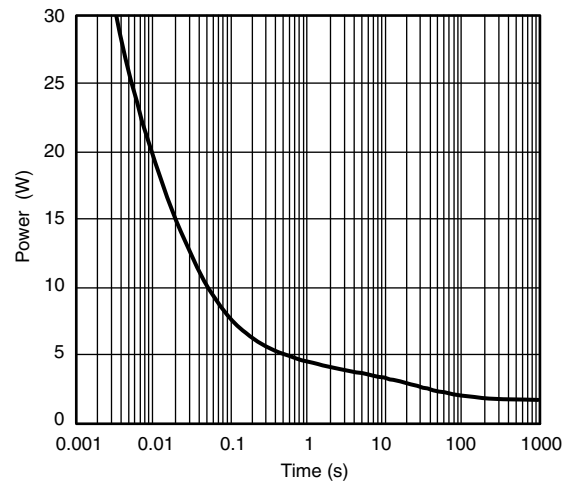
Source-Drain Diode Forward Voltage



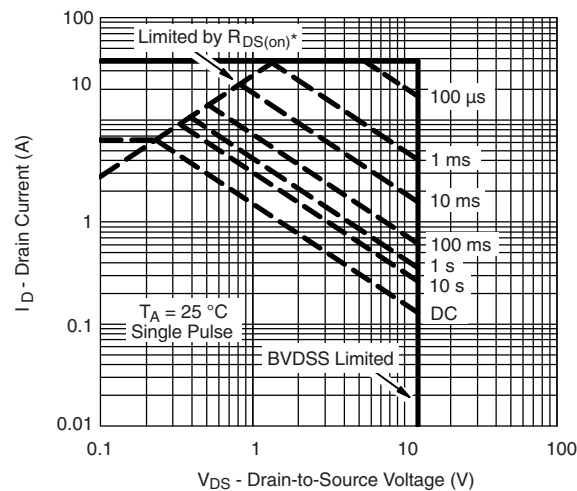
On-Resistance vs. Gate-to-Source Voltage



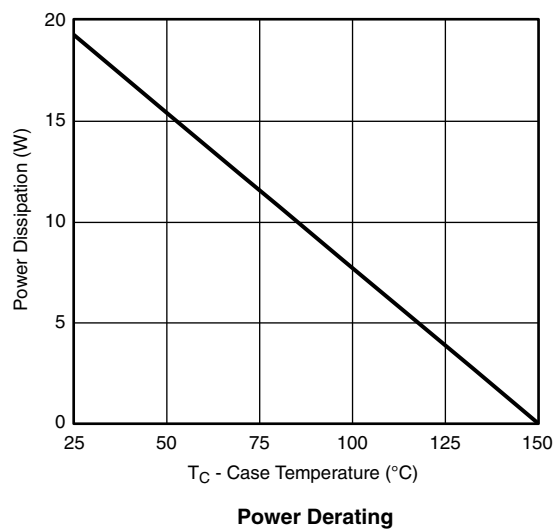
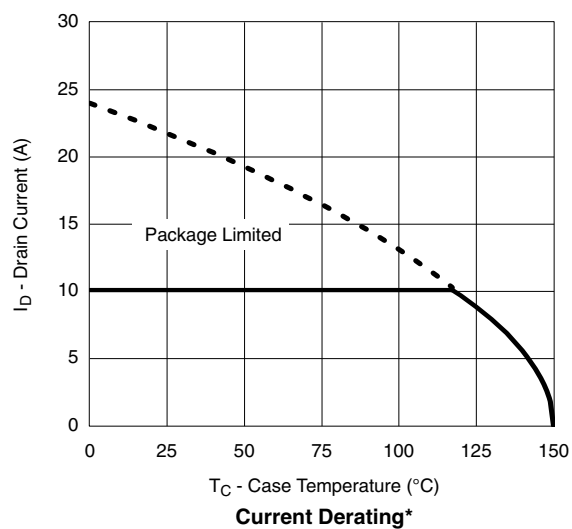
Threshold Voltage



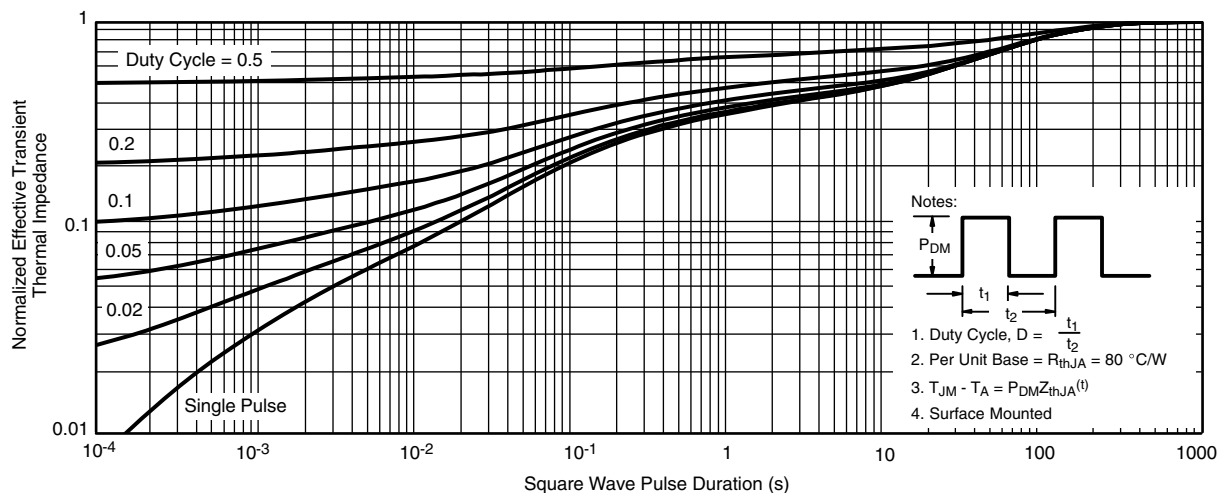
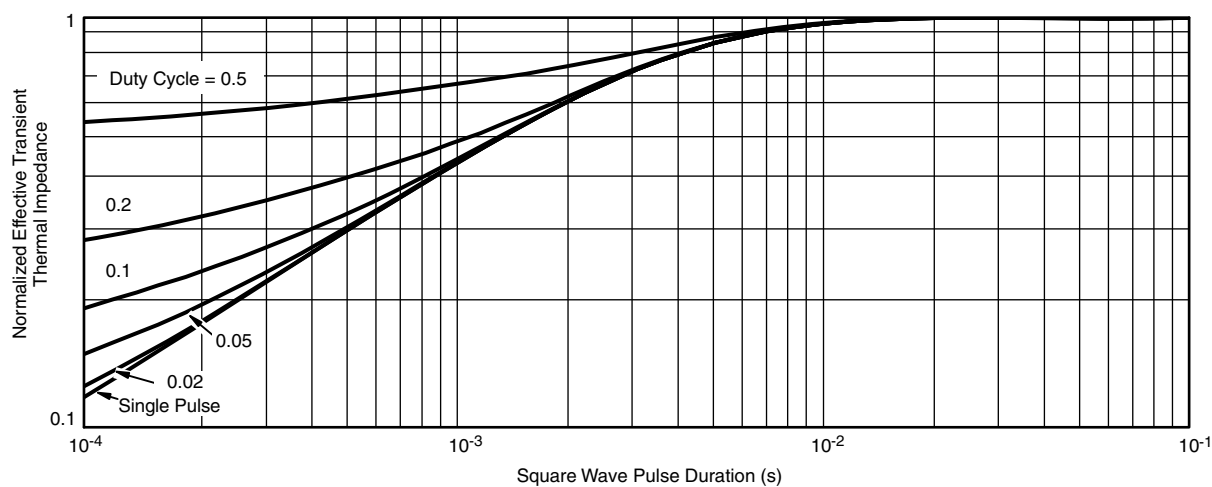
Single Pulse Power, Junction-to-Ambient



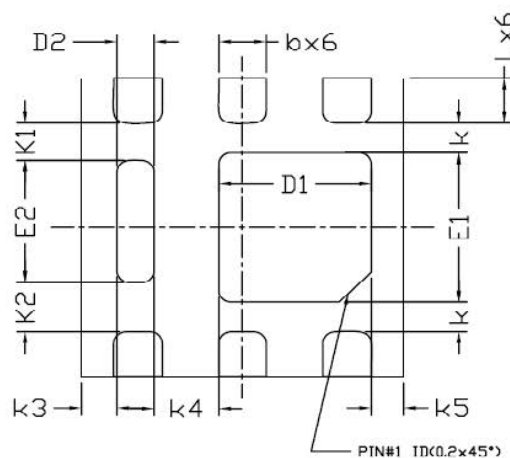
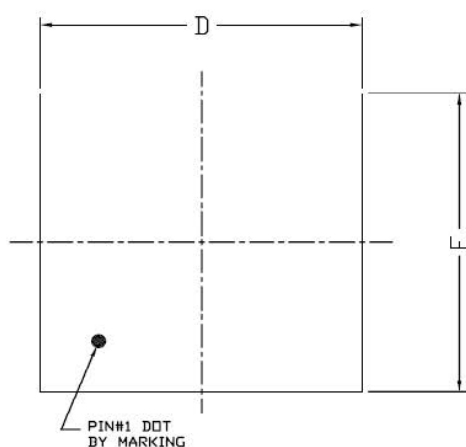
Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

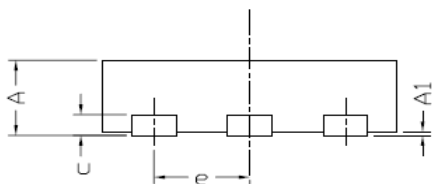
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

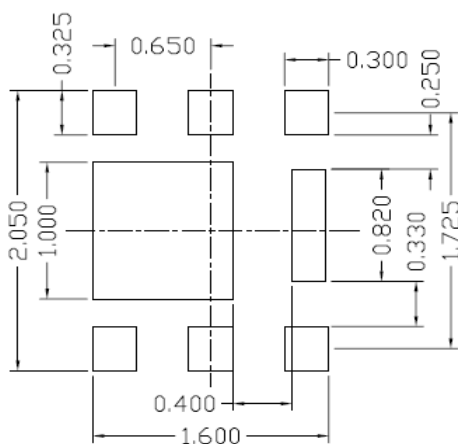
## DFN2x2 \_6L\_EP1\_S PACKAGE OUTLINE



BOTTOM VIEW



## RECOMMENDED LAND PATTERN



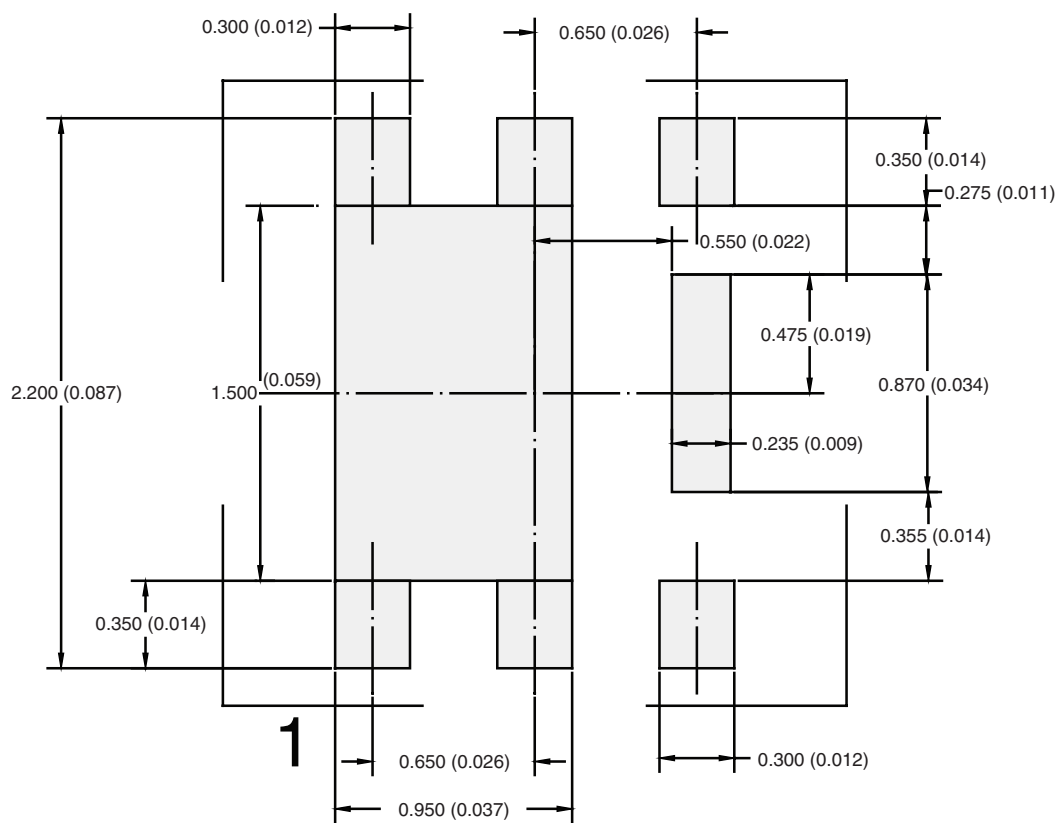
UNIT: mm

## NOTE

1. CONTROLLING DIMENSION IS MILLIMETER.  
 CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.152 REF			0.006 REF		
D	1.90	2.00	2.10	0.075	0.079	0.083
D1	0.85	0.95	1.05	0.033	0.037	0.041
D2	0.13	0.23	0.33	0.005	0.009	0.013
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	0.90	1.00	1.10	0.035	0.039	0.043
E2	0.72	0.82	0.92	0.028	0.032	0.036
e	0.65 BSC			0.026 BSC		
K	0.20 BSC			0.008 BSC		
K1	0.25 BSC			0.010 BSC		
K2	0.33 BSC			0.013 BSC		
K3	0.22 BSC			0.009 BSC		
K4	0.40 BSC			0.016 BSC		
K5	0.20 BSC			0.008 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014

## RECOMMENDED PAD LAYOUT FOR DFN2X2



Dimensions in mm/(Inches)



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